GENERAL CHAIR'S GREETING

On behalf of the conference committee, I am pleased to invite you to the 2003 IEEE International Silicon on Insulator (SOI) Conference. As with previous conferences, the 2003 SOI Conference continues to provide a forum for the interaction of scientists and engineers interested in all aspects of SOI technologies. This year will feature an outstanding Technical Program, a one-day Short Course that will precede the Technical Program, and an Industrial Exhibit with participation from SOI suppliers, SOI equipment manufacturers, device simulation services, and devices manufacturers.

The Technical Program Committee, chaired by Mike Mendicino (Motorola/USA), has worked hard to select an outstanding set of papers to broaden the perspective of the active specialists with new information and to provide the necessary background for the newcomers in the field. Three invited speakers will lead off the conference with the Plenary Session on Tuesday.

This year's Short Course is The DESIGN OF SOI DEVICES BASED ON PHYSICS. Presented Monday, September 28th, four specialists in the field will provide knowledge for better device design, better utilization of new physical phenomena, and to break through the technical barriers into nano-scale technology. Organized by Toshiro Hiramoto of the Tokyo University, the Short Course promises to be an exciting addition to the conference.

The Rump Session (panel discussion) on SOI-SOC will follow the Cookout Wednesday evening. Organized by Pierre Fazan (EPFL, Switzerland) the panel will consist of six panelists from Europe, Asia, and North America. Questions and discussion will follow the short panel presentation on RF, mixed mode, embedded dense memories, and high performance logic on SOI.

The friendly and informal atmosphere that contributes to the success of our conference year after year is enhanced by a number of social events for attendees and their guests. Our social program begins with a welcome reception on Monday evening September 29th. On Tuesday night, after the poster session, the conference banquet will take place. Dr. Bruce Betts of the Planetary Society will be our banquet speaker. He will enlighten us on "Red Rover Goes to Mars: Engaging the Public in Mars Exploration."

Finally, I would like to express my sincere thanks to you, the author and the participant, for making the conference successful. I would also like to express my sincere thanks to the executive and technical committees and the conference management for putting together this excellent program.

We look forward to seeing you in Newport Beach, California.

Sincerely,
Michael S.T. Liu, General Chairman

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29TH ANNUAL IEEE INTERNATIONAL SOI CONFERENCE

EXECUTIVE COMMITTEE

GENERAL CHAIR
Mike Liu, Honeywell International
Tel: (763)954-2361 • Fax: (763)954-2504
Email: mike.s.liu@honeywell.com

MICHAEL S. LIU, received his Ph.D in electrical engineering from the University of Minnesota in 1967 and joined Honeywell in 1968. He is a chief fellow at Honeywell SSEC (DES/Plymouth). He is an author/co-author of over 100 papers in three areas: ferroelectric materials and pyroelectric detectors technology, selective epitaxial and lateral overgrowth technology, and SOI materials and SOI CMOS technology. He holds 18 US patents. His current interests are thin SOI materials, total dose radiation effects and single event effects in deep sub-micron SOI CMOS devices. He is a senior member of IEEE and was a general chair for the 1979 IEEE Symposium on Applications of Ferroelectrics.

TECHNICAL SESSION CHAIR
Michael Mendicino, Motorola
Tel: 512.933-7283 8 Fax: 512.933-5304
Email: RA1458@email.sps.mot.com

MIKE MENDICINO received his B.S. degree from Ohio State University in 1989, and his M.S. and Ph.D. degrees in chemical engineering from the University of Illinois in 1994. He completed a two-year assignment at SEMATECH where he was a project leader responsible for thin film SOI materials characterization and development. He is currently with Motorola's Digital DNA Laboratories working on advanced device technologies for high performance CMOS applications. Mike is a fellow of the technical staff at Motorola and member of IEEE.

LOCAL ARRANGEMENTS CHAIR
James Burns, MIT Lincoln Labs
Advanced Silicon Technology
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Email: jab@ll.mit.edu

JAMES A. BURNS received his B.S. in physics from Carnegie Institute of Technology (1960) and his Ph.D. in physics from the University of Vermont (1975). He worked in semiconductor and magnetic film device design and processing at IBM and CCD design while at Honeywell. Since 1975 he has been a staff member at MIT's Lincoln Laboratory where his principal interests are silicon transistor and process design and the development of analytical techniques to customize IC fabrication to integrated circuit applications. He developed the laboratory's deep submicron fully depleted SOI process and is currently working on integrating that SOI technology into a 3-dimensional integrated circuit technology. He is a member of the American Physical Society, IEEE, and Tau Beta Pi.

TREASURER
Christophe Tretz, IBM, San Jose Design Center
Tel: 408.888.3852 • Email: ctretz@us.ibm.com

CHRISTOPHE TRETZ received his B.Sc. degree (1991) from the Ecole Nationale Superieure d'Electronique, Electrotechnique, Informatique et Hydraulique de Toulouse, France, and his M.S. (1992) and Ph.D. in electrical engineering (1997) from Columbia University, New York. He joined IBM at the TJ Watson Research Center in Yorktown Heights, NY in 1997 where he contributed to the design of several microprocessors for servers and workstations both with bulk and SOI processes. In 2000, he joined the technical staff of Advanced Micro Devices, California Microprocessor Division, where he contributed to the design of the Hammer microprocessor family and established design guidelines for microprocessor using SOI technologies.

He is now back with IBM as a senior circuit design engineer in the San Jose Design Center, Engineering and Technology Services Division. Dr. Tretz has authored/coauthored about 20 papers and three US patents in the field of circuit design techniques using SOI, circuit optimization and low power design. His current research interests remain in optimizing circuit design for SOI and in improving design choices for SOI.

SENIOR CONFERENCE COMMITTEE

RUMP & POSTER CHAIR
Pierre C. Fazan, EPFL, STI/IMM/LEG.EPFL
Tel: 41 21 693 4604 • Fax: 41 21 693 3640
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PIERRE C. FAZAN was born in Lausanne, Switzerland where he earned his physics diploma and Ph.D. degrees at the Swiss Federal Institute of Technology (EPFL) in 1984 and 1988 respectively. From 1989 to 1997 he worked as process integration engineer then manager at Micron Technology, Boise Idaho, USA, focusing on DRAM process integration. In 1997 he was named Professor at the Swiss Federal Institute of Technology, Lausanne, EPFL. In 1999 he founded Innovative Silicon Solutions, a consulting company specialized in embedded memory design and integration. In 2002 he co-founded Innovative Silicon S.A., an IP startup developing a new SOI single transistor memory concept. He authored/co-authored more than 95 papers and invented/co-invented more than 140 US patents. Dr. Fazan has served as member in program committees of IEDM, VLSI Tech. Symp, ISIF, ESSDERC, INFOS and ECS Conferences.

SHORT COURSE CHAIR
Toshiro Hiramoto, University of Tokyo
Institute of Industrial Science
Tel: 81 3 5452-6263
Emil: hiramoto@nano.iis.u-tokyo.ac.jp

TOSHIRO HIRAMOTO received his B.S., M.S., and Ph.D degrees in electronic engineering from the University of Tokyo in 1984, 1986, and 1989, respectively. In 1989, he joined Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in the device and circuit design of ultra-fast BiCMOS SRAMs. In 1994, he joined the Institute of Industrial Science, University of Tokyo, Japan, as associate professor. He was also an associate professor at the VLSI Design and Education Center, University of Tokyo, from 1996 to 2002. He has been a professor at the Institute of Industrial Science, University of Tokyo since 2002. His research interests include low power and low voltage design of advanced CMOS devices, SOI MOSFETs, device/circuit cooperation

scheme for low power VLSI, quantum effects in nano-scale MOSFETs, and silicon single electron transistors. Dr. Hiramoto is a member of IEEE, IEICE, and Japan Society of Applied Physics. He has been an Elected AdCom Member of IEEE Electron Devices Society since 2001. He served as the program chair of Silicon Nanoelectronics Workshop in 1997, 1999, and 2001, and as the general chair of the Silicon Nanoelectronics Workshop in 2003.

PUBLICITY CHAIR
R. V. JOSHI, IBM Research Division
TJ Watson Research Center
Tel: 914.945.1118 • Fax: 914.945.2141
Email: rvjoshi@us.ibm.com

Dr. Rajiv V. Joshi is a research staff member at TJ Watson Research Center, IBM. He received his B.Tech degree from Indian Institute of Technology (Bombay, India), M.S degree from Massachusetts Institute of Technology and Ph.D. in engineering science from Columbia University, New York. He was with GTE research lab in Waltham, Massachusetts from 1981 to 1983. He joined IBM in 1983 and since then has worked in VLSI design systems, science and technology. He worked on 1.25µm NMOS, and CMOS, sub-0.5µm CMOS logic, DRAM and SRAM technologies. He developed novel interconnect processes and structures for Aluminum, tungsten and Copper technologies which are widely used in IBM for various sub-0.5µm memory and logic technologies as well as across the globe. His circuit related work includes design of register files, registers, latches, L1 caches, Directory, TLB, IO circuits development of physical design tools, and CAD based library generation and circuit designs in SOI technology. He contributed to S/390 Alliance processor design, working in both circuit design and CAD tools. The Alliance G5 chip was a very successful IBM product and Joshi received IBM Research Division Awards for his contributions to it and each of the follow-on processor designs. His 2 GHz SRAM design for G6 received an Outstanding Technical Achievement Award. His work also involved design related to SRAM designs, which are widely used across IBM System 390. He has won 26 Invention Plateau Achievement awards from IBM and won two Patent Portfolio awards for cross-licensing and utilization of his patents in the IBM products. He has received five Research Division awards, and several top 5% and top 30% patent awards (for licensing activities). On June 6, 2002 he received Corporate Patent Portfolio award from IBM. He is a master inventor and key technical leader at IBM research

division. He has authored/co-authored over 95 research papers and presented several invited talks. He holds 60 U.S. patents in addition to 40 pending patents. He received the Lewis Winner Award in 1992 for an outstanding paper he co-authored at the International Solid State Circuit Conference. He was instrumental in starting interconnect workshop in early 1980s. He chaired advanced interconnect conferences sponsored by MRS and served as an editor of the proceedings. He is elected as an IEEE fellow for 2002 for contributions to chip metallurgy materials and processes, and high performance processor and circuit design. He is actively involved in IEEE ISLPED (Int. Symposium Low Power Electr. Design) IEEE VLSI design, IEEE Int. SOI conf Program committees.

● ● TECHNICAL COMMITTEE ● ●

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Harry Hovel, IBM Corporation
Dimitris Ioannou, George Mason University
Jason Woo, UCLA

SHORT COURSE OVERVIEW

The theme of this year's short course is the design of SOI devices based on physics. The size of MOS devices, including SOI MOSFETs, is rapidly shrinking and rushing into the nanoscale regime where it is highly probable we will confront a variety of technological barriers. At the same time, various types of new physical phenomena that have not been considered in the micrometer scale, have manifested themselves in device characteristics. In order to overcome this crisis, we have to return to the most fundamental understanding of physics. We certainly need more profound knowledge of physics for better device design than ever before, and it is expected that the positive utilization of new physical phenomena will open a way to break the technological barriers.

The objective of the course is to give attendees a basic idea of physics for better design of nanoscale MOSFETs. Issues to be addressed include mobility in bulk and SOI MOSFETs, ways to design strained silicon and strained SOI MOSFETs, transport mechanisms without any scattering, and scaling limit that may be also determined by the nanoscale physics. The materials presented will provide an idea of physics-based design of devices and will help us to expand the outlook of future device technology.

SHORT COURSE AGENDA

7:00am - 5:00pm	Registration
7:00am - 8:00am	Continental Breakfast
8:25am - 8:30am	**Introduction,** *T. Hiramoto*
8:30am - 10:00am	**Mobility in bulk and SOI MOSFETs** *J. Koga, Toshiba*
10:00am - 10:15am	Break
10:15am - 11:45am	**Mobility and Device Design in Strained Si and Strained-SOI MOSFETs** *J. Hoyt, MIT*
12:00pm - 1:30pm	Hosted Lunch
1:30pm - 3:00pm	**Ballistic Transport in SOI MOSFETs** *M. Lundstrom, Purdue University*
3:00pm - 3:15pm	Break
3:15pm - 4:45pm	**Scaling Limits of Bulk & SOI MOSFETs** *D. Frank, IBM*
4:45pm - 5:00pm	Course Wrap-up
6:00pm - 8:00pm	Welcome Reception

SHORT COURSE INSTRUCTORS

JUNJI KOGA received his B.S. degree in physics from the University of Tokyo, Japan, in 1988. He joined the Research and Development Center of Toshiba Corporation, Kawasaki, Japan, in 1988, where he has been engaged in the research on the device physics of Si MOSFET including the carrier transport in the inversion layer for both bulk and thin-film SOI transistors, Cryo-CMOS device technology, and silicon functional tunnel device such as negative differential conductance device and single electron device. He is now with Advanced LSI Technology Laboratory of Toshiba Corporation. He serves on the technical program committee at the International Electron Devices Meeting. He is a member of the Japan Society of Applied Physics.

MARK LUNDSTROM earned his B.E.E. and M.S.E.E. degrees from the University of Minnesota in 1973 and 1974 and his Ph.D. from Purdue University in 1980. He joined Purdue University in 1980 where he is the Scifres Distinguished Professor of Electrical and Computer Engineering and Director of the National Science Foundation Network for Computational Nanotechnology. Before attending Purdue, he worked at Hewlett-Packard Corporation on NMOS process development and manufacturing. His current research interests focus on the physics and technology of nanoscale devices. Lundstrom is a fellow of both the Institute of Electrical and Electronic Engineers (IEEE) and the American Physical Society and the recipient of several awards for his teaching and research, most recently IEEE's 2002 Cledo Brunetti Award for his work on nanoscale electronics.

DAVID J. FRANK received his B.S. from the California Institute of Technology, Pasadena, CA in 1977 and a Ph.D. in physics from Harvard University, Cambridge, MA in 1983. Since graduation Dr. Frank has been employed at the IBM TJ Watson Research Center, Yorktown Heights, NY, where he is a Research Staff Member. His studies have included non-equilibrium superconductivity, modeling and measuring III-V devices, and exploring the limits of scaling of silicon technology. His recent work includes the modeling of innovative Si devices, analysis of CMOS scaling issues such as power consumption, discrete dopant effects and short-channel effects associated with high-k gate insulators, investigating the usefulness of energy-recovering CMOS logic and reversible computing concepts, and low power circuit design. Dr. Frank is an IEEE Fellow and has served on technical program committees for the International Electron Devices Meeting and the Si Nanoelectronics Workshop. He has authored/co-authored over 80 technical publications and holds seven U.S. patents.

JUDY L. HOYT received her B.S. degree in physics and applied mathematics from the University of California, Berkeley in 1981, and his Ph.D. degree in applied physics from Stanford University in 1987. From 1988 through 1999 Dr. Hoyt was on the electrical engineering research staff at Stanford University. In January 2000, she became a faculty member in Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA. Dr. Hoyt pioneered the development of strained Si MOSFET technology in the early 1990s. Her primary research interests are in the areas of novel silicon-based heterostructure and nanostructure devices, new processes and materials for advanced device applications, Si epitaxy and chemical vapor deposition, CMOS front-end processing, and three-dimensional integration. She has authored/co-authored 80 publications in these areas, and holds four patents. Dr. Hoyt received the IEEE Electron Devices Society Rappaport Award in 1990. She has served as general chair of the IEEE International Electron Devices Meeting (2001), and is a member of the Electron Devices Society, the American Physical Society, and the Materials Research Society.

PROGRAM SCHEDULE AT-A-GLANCE

REGISTRATION	Sunday, September 28	6:00pm – 8:00pm
	Monday, September 29	7:00am – 5:00pm
	Tuesday, September 30	7:00am – 5:00pm
	Wednesday, October 1	7:00am – 12:00pm
	Thursday, October 1	7:00am – 12:00pm
EXHIBITS OPEN	Tuesday, September 30	3:40pm – 8:00pm
	Wednesday, October 1	8:00am – 12:00pm
	Thursday, October 2	8:00am – 12:00pm

CONFERENCE SCHEDULE

MONDAY, September 29

7:00am	Short Course Breakfast
8:00am	Short Course
12:00pm	Short Course Lunch
1:30pm	Short Course
6:00pm	Welcome Reception

TUESDAY, September 30

7:00am	Continental Breakfast
8:00am	Introduction & Welcome
8:15am	**Session 1:** PLENARY SESSION
10:20pm	Break
10:40am	**Session 2:** CIRCUIT TECHNIQUES AND APPLICATIONS I
12:40pm	Lunch
1:40pm	**Session 3:** PROCESS AND DEVICE TECHNOLOGY
3:40pm	**Session 4:** POSTER SESSION
6:30pm	Banquet Reception
7:00pm	Banquet

WEDNESDAY, October 1st

7:00am	Continental Breakfast
8:00am	**Session 5:** CIRCUIT TECHNIQUES AND APPLICATIONS II
10:00am	Break
10:20am	**Session 6:** NOVEL DEVICES
12:20pm	Lunch & Activities
6:30pm	Cookout Dinner
8:00pm	Rump Session

THURSDAY, October 2nd

7:00am	Continental Breakfast
8:00am	**Session 7:** SOI MATERIALS TECHNOLOGY AND CHARACTERIZATION
10:00am	Break
10:20am	**Session 8:** DEVICE DESIGN AND CHARACTERIZATION
12:20pm	Lunch
1:20pm	**Session 9:** SOI DEVICE EFFECTS AND CIRCUIT IMPACT
3:00pm	Break
3:20pm	**Session 10:** LATE NEWS
5:25pm	Wrap-up & Presentation of Best Paper Award

***THE TECHNICAL PROGRAM** will consist of 42 oral and 20 poster papers, as well as three invited talks. Technical Sessions and Session chairs are as follows.*

Session 1	**PLENARY** *Chair: Michael Mendicino*
Session 2	**CIRCUIT TECHNIQUES AND APPLICATIONS** *Chairs: Hector Sanchez, Rajiv Joshi*
Session 3	**PROCESS AND DEVICE TECHNOLOGY** *Chairs: Samuel Fung, James Burns*
Session 4	**POSTERS** *Chair: Pierre Fazan*
Session 5	**CIRCUIT TECHNIQUES AND APPLICATIONS II** *Chairs: Christophe Tretz, Ted Houston*
Session 6	**NOVEL DEVICES** *Chairs: Gerold Neudeck, Daniel Radack*
Session 7	**SOI MATERIALS TECHNOLOGY AND CHARACTERIZATION** *Chairs: George Cellar, Atsushi Ogura*
Session 8	**DEVICE DESIGN AND CHARACTERIZATION** *Chairs: Toshiro Hiramoto, Jean-Pierre Colinge*
Session 9	**SOI DEVICE EFFECTS AND CIRCUIT IMPACT** *Chairs: Olivier Faynot, Dimitris Ioannou*
Session 10	**LATE NEWS** *Chair: Mike Liu*

TECHNICAL PROGRAM SCHEDULE

Tuesday, September 30

SESSION 1 PLENARY SESSION
Chair: Michael Mendicino

8:15am 1.1 SOI nano-technology for high-performance system on-chip applications
Dr. Jean-Olivier Plouchart, IBM T.J. Watson Research Center

8:55am 1.2 Ultra-low voltage MTCMOS/SOI circuits for batteryless wireless system
Dr. Takakuni Douseki, NTT

9:35am 1.3 Photonic bandgap microcavities and waveguides
Dr. Axel Scherer, M. Loncar, T. Yoshie, K. Okamoto; California Institute of Technology

SESSION 2 CIRCUIT TECHNIQUES AND APPLICATIONS I
Chairs: Hector Sanchez, Rajiv Joshi

10:40am 2.1 A new block refresh concept for SOI floating body memories
P. Fazan[1,2], S. Okhonin[1,2], M. Nagoga[1,2]; [1]Swiss Federal Institute of Technology [2]Innovative Silicon S.A.

11:00am 2.2 Potential of SOI intrinsic MOSFETs for ring VCO design
D. Levacq, L. Vancaillie, D. Flandre; Université catholique de Louvain

11:20am 2.3 Ultra low-power design techniques using special SOI MOS diodes
D. Levacq[1], C. Liber[1], V. Dessard[2], D. Flandre[1]; [1]Université catholique de Louvain, [2]CISSOID

11:40am 2.4 A low power four transistor Schmitt Trigger for asymmetric double gate fully depleted SOI devices
Tamer Cakici, Aditya Bansal, Kaushik Roy; School of ECE, Purdue University

12:00pm 2.5 Human body model ESD protection concepts in SOI and bulk CMOS at the 130nm node
C. Putnam[1], R. Gauthier[1], M. Muhammad[1], K. Chatty[1], M. Woo[2]; [1]IBM Microelectronics Semiconductor Research & Development Center, [2]OAO Services, Inc.

12:20pm 2.6 Proton induced single event upset in a 4M SOI SRAM
H.Y. Liu[1], K.W. Golke[1], D.K. Nelson[1], W.W. Heikkila[1], S.T. Liu[1], W.C. Jenkins[2]; [1]Honeywell, [2]Naval Research Laboratory

SESSION 3 PROCESS AND DEVICE TECHNOLOGY
Chairs: Samuel Fung, James Burns

1:40pm 3.1 Fully-depleted SOI process optimization for 60nm CMOS transistors
C. Fenouillet-Beranger[2], F. Fruleux[1], A. Talbot[1], L. Tosti[2], R. Palla[1], M. Cassé[2], N. Carriere[2], P. Mazoyer[1], A. Grouillet[2], C. Raynaud[2], B. Giffard[2], T. Skotnicki[1]; [1]ST Microelectronics, [2]CEA LETI

2:00pm 3.2 FinFET technology for future microprocessors
T. Ludwig[1], I. Aller[1], V. Gernhoefer[1], J.Keinert[1], E. Nowak[2], R.V. Joshi[3], A. Mueller[1], S. Tomaschko[1]; [1]IBM Deutschland, [2]IBM Microelectronics Division, [3]IBM Research

2:20pm 3.3 High resolution 2D Scanning Spreading Resistance Microscopy (SSRM) of thin film SOI MOSFETs with ultra short effective channel length
J. Hartwich[1], D. Alvarez[1,2], L. Dreeskornfeld[1], F. Hofmann[1], J. Kretz[1], E. Landgraf[1], R.J. Luyken[1], W. Rösner[1], T. Schulz[1], M. Specht[1], M. Städele[1], W. Vandervorst[2], L. Risch[1]; [1]Infineon Technologies AG, [2]IMEC

2:40pm 3.4 High performance partially depleted SOI using spike RTA
Laegu Kang, Paul Grudowski, Veer Dhandapani, Yongjoo Jeon, Sinan Goktepeli, Byoung Min, Geoffrey Yeap, Mark Foisy, Steven Anderson, Michael Mendicino, Suresh Venkatesan; Motorola, Inc.

3:00pm 3.5 Elimination of parasitic channels in fully depleted SOI CMOS

C.K. Chen, C.L. Chen, P.W. Wyatt, P.Gouker, J.A. Burns, D.R.W. Yost, V. Suntharalingam, C.L. Keast; Lincoln Laboratory, Massachusetts Institute of Technology

3:20pm 3.6 Effects of SOI film thickness on high-performance microprocessor by 0.13 um partially depleted SOI CMOS technology

Jianan Yang, Byoung Min, Yasuhito Shiho, Laegu Kang, Phil Walker, Michael Mendicino, Geoffrey Yeap, Mark Foisy, Kevin Cox, Jim Cartwright, Suresh Venkatesan; Motorola, Inc.

SESSION 4 POSTERS

3:40pm *Chair: Pierre Fazan*

P1 SGOI thinning and uniformity improvement using a fluoride GCIB process

J.O. Chu[1], L.P. Allen[2], W. Skinner[2], J. Hautala[2], T.G. Tetreault[2], R. MacCrimmon[2], C. Santeufemio[2], E. Degenkolb[2], D.B. Fenner[2]; [1]IBM T.J. Watson Research Center, [2]Epion Corporation

P2 Surface smoothing effect in patterned SOI fabrication with SIMOX technology

T. Sasaki, S. Takayama, K. Kawamura, T. Maeda, Y. Nagatake, A. Matsumura; Wacker NSCE Corp.

P3 High resistivity SOI substrates: how high should we go?

D. Lederer[1], C. Desrumeaux[2], François Brunier[2], J.P. Raskin[1]; 1Microwave Laboratory of UCL, [2]SOITEC

P4 Photon back-scatter analysis of SOI wafers

Rene P. Zingg[1], Fred D. Orazio[2]; [1]Philips Semiconductors, [2]VTI Inc.

P5 The G4-FET: low voltage to high voltage operation and performance

B. Dufrene[1], K. Akarvardar[2], S. Cristoloveanu[2], B. Blalock[1], P. Fechner [3], M. Mojarradi [4]; [1]The University of Tennessee, [2]Institute of Microelectronics, Electromagnetism, and Photonics (UMR CNRS), ENSERG, [3]Honeywell SSEC, [4]Jet Propulsion Laboratory

P6 A Novel Photodiode-type active pixel sensor utilizing DTMOS with reduced fixed-pattern noise

Mamoru Terauchi; Hiroshima City University

P7 Silicon single crystal on quartz: fabrication and benefits

François Brunier[1], O. Rayssac[1], I. Cayrefourcq[1], Hideaki Oka[2], Takashi Sato[2], Franck Fournel[3], Chrystelle Lagahe[3]; [1]SOITEC, [2]SEIKO EPSON, [3]CEA-DRT, LETI-DTS, CEA-GRE

P8 Effect of nano-scale strained Si grown on SiGe-on-Insulator on electron mobility

J.G. Park[1], T.H. Shim[1], T.H. Lee[1], Y.K. Park[1], H.K. Moon[1], S.L. Maeng[2], W.J. Cho[2], S.D. Yoo[3]; [1]Hanyang University, [2]Electronic and Telecommunications Research Institute, [3]Hynix Semiconductor, Inc.

P9 A novel local bottom-gate carbon nanotube field effect transistor on SOI

Min Zhang, Philip C.H. Chan, Qi Liang, Zikang Tang; Hong Kong University of Science and Technology

P10 Accumulation-mode Pi-gate MOSFET

J.W. Park[1], J.P. Colinge[2]; [1]Kumoh National University of Technology, [2]University of California, Davis

P11 Design of DG-MOSFETs for high linearity performance

S. Kaya[1], W. Ma[1], A. Asenov[2]; [1]SSECS, Ohio University, [2]University of Glasgow

P12 NiSi MOCVD for fabricating FinFETs and UTB-SOI devices

Atsushi Ogura[1], Hitoshi Wakabayashi[1], Masato Ishikawa[2], Takeshi Kada[2], Hideaki Machida[2], Yoshio Ohshita[3]; [1]NEC Corporation, [1]Tri Chemical Laboratories, Inc., [3]Toyota Technological Institute

P13 Optimizing the salicide thickness for improving 130nm PD SOI performance

S. Haendler[1,3], R. Gwoziecki[1,2], C. Tabone[2], H. Brut[1], C. Raynaud[1,2]; [1]ST Microelectronics, [2]LETI , [3]IMEP

P14 Charge pumping effects in partially depleted SOI MOSFETs

S. Okhonin[1,2], M. Nagoga[1,2], P. Fazan[1,2]; [1]Swiss Federal Institute of Technology, [2]Innovative Silicon S.A.

P15 Frequency degradation of SOI MOS device output conductance

D. Lederer, M. Dehan, D. Vanhoenacker, J.P. Raskin; Microwave Laboratory of UCL

P16 Peculiarities of the temperature behavior of SOI MOSFETs in the deep submicron area

L. Vancaillie[1], V. Kilchytska[1], P. Delatte[2], L. Demeüs[2], H. Matsuhashi[3], F. Ichikawa[3], D. Flandre[1]; 1Université catholique de Louvain, Microelectronics Lab, [2]CISSOID, [3]OKI Electric Industry Co., Ltd.

P17 Modeling isolation-induced mechanical stress effect on SOI MOS devices

K.W. Su, K.H. Chen, H.Y. Chen, C.Y. Chang, S.J. Yang, Y.M. Sheu, T. Tsao, F.L. Yang, J.K. Her; TSMC

P18 Minimizing the floating body induced SEU sensitivity in a 0.35µ SOI SRAM cell through recombination lifetime control

D.P. Ioannou[1], S. Mitra[1], D.E. Ioannou[1], S.T. Liu[2], W.C. Jenkins[3]; [1]George Mason Univ., [2]Honeywell SSEC, [3]Naval Research Laboratory

P19 Micropower, 0.35µm partially depleted SOI CMOS preamplifiers having low white and flicker noise

D. M. Binkley[1], D.H. Ihme[1], B.J. Blalock[2], M.M. Mojarradi[3]; [1]University of North Carolina, [2]University of Tennessee, [3]Jet Propulsion Laboratory, California Institute of Technology

P20 Noise considerations and detailed comparison of low standby gate/sub-threshold leakage digital circuits in nano-scale SOI technology

Koushik K. Das[1], Rajiv V. Joshi[2], Ching-Te Kent Chuang[2], Richard B. Brown[1]; [1]University of Michigan, [2]IBM, TJ Watson Research Center

7:00pm **Banquet**

Wednesday, October 1

SESSION 5 CIRCUIT TECHNIQUES AND APPLICATIONS II

Chairs: Christophe Tretz, Ted Houston

8:00am 5.1 Stand-by current in PD-SOI Pseudo-nMOS circuits

Jayakumaran Sivagnaname, Richard B. Brown; University of Michigan

8:20am 5.2 Double gate MOSFET subthreshold logic for ultra-low power applications

Jae-Joon Kim, Kaushik Roy; School of ECE, Purdue University

8:40am 5.3 Analysis of the impact of gate-body signal phase on DTMOS inverters in 0.13µm PD-SOI

Alan J. Drake[1], Noah Zamdmer[2], Kevin J. Nowka[3], Richard B. Brown[1]; [1]University of Michigan, [2]IBM Microelectronics Semiconductor Research and Development Center, [3]IBM Austin Research Lab

9:00am 5.4 New process and pixel structure of an SOI-CMOS imager

Xinyu Zheng[1], Suresh Seshadri[1], Michael Wood[2], Chris Wrigley[1], Bedabrata Pain[1]; [1]Jet Propulsion Laboratory, California Institute of Technology, [2]Space and Naval Warfare Systems Center (SPAWAR)

9:20am 5.5 A CMOS active pixel sensor on silicon-on-sapphire substrate with backside illumination

Chao Shen[1], Chen Xu[1], Ru Huang[2], Ping K. Ko[1], Mansun Chan[1]; [1]Hong Kong University of Science and Technology, [2]Institute of Microelectronics, Peking University

9:40am 5.6 Scaled front-side and back-side trapping SONOS memories on SOI

H. Silva[1], M.K. Kim[2], C.W. Kim[2], S. Tiwari[1]; [1]Cornell University, [2]Samsung Advanced Institute of Technology

SESSION 6 **NOVEL DEVICES**

Chairs: Gerold Neudeck, Daniel Radack

10:20am 6.1 Finfet with isolated n+ and p+ gate regions strapped with metal and polysilicon

L. Mathew[1], M. Sadd[1], B.E. White[1], A. Vandooren[1], S. Dakshina-Murthy[2], J. Cobb[1], T. Stephens[1], R. Mora[1], D. Pham[1], J. Conner[1], T. White[1], Z. Shi[1], A. V-Y Thean[1], A. Barr[1], M. Zavala[1], J. Schaeffer[1], M.J. Rendon[1], D. Sing[1], M. Orlowski[1], B.Y. Nguyen[1], J. Mogab[1]; [1]APRDL, [2]Motorola–AMD Alliance

10:40am 6.2 Corner effect in multiple-gate SOI MOSFETs

W. Xiong[1], J.P. Colinge[2]; [1]Sematech, [2]University of California, Davis

11:00am 6.3 The pH response of a Silicon-on-Insulator MOSFET with an integrated nanofluidic cell

B. R. Takulapalli, T.J. Thornton, B. Ashcroft, S.M. Lindsay, H.Q. Zhang, N.J. Tao, D. Gust; Arizona State University

11:20am 6.4 Optically tunable narrowband filter using defect-induced pass-band in photonic crystal waveguide

Yukio Iida, Yasuhisa Omura, Masataka Tsuji; Kansai University

11:40am 6.5 Control of threshold voltage and short channel effects in ultra-thin Strained-SOI CMOS

Toshinori Numata, Tomohisa Mizuno, Tsutomu Tezuka, Junji Koga, Shin-ichi Takagi; MIRAI Project, ASET

12:00pm 6.6 Short channel and back-gate coupling effects in Silicon-On-Nothing (SON) MOSFETs

J. Pretet[1,2], S. Cristoloveanu[2], T. Skotnicki[1], S. Monfray[1]; [1]ST Microelectronics, [2]IMEP (UMR CNRS/INPG/UJF), ENSERG

12:45pm **Lunch and Afternoon Activities**

6:30pm **Cookout**

8:00pm **Rump Session**

Thursday, October 2

SESSION 7 **SOI MATERIALS TECHNOLOGY AND CHARACTERIZATION**

Chairs: George Cellar, Atsushi Ogura

8:00am 7.1 SOI wafer polishing with magnetorheological finishing (MRF)

Marc Tricard, Paul R. Dumas, Don Golini, James T. Mooney; QED Technologies

8:20am 7.2 Formation of strained Si/GiGe on insulator structure with a (110) surface

N. Sugiyama, T. Mizuno, Y. Moriyama, S. Nakaharai, T. Tezuka, S. Takagi; MIRAI Project, ASET

8:40am 7.3 Systematic study of the splitting kinetic of H/He co-implanted substrate

Phuong Nguyen[1], I. Cayrefourcq[1], B. Blondeau[1], N. Sousbie[1], C. Lagahe-Blanchard[2], S. Sartori[2], A.M. Cartier[2]; [1]SOITEC SA, [2]CEA–DRT–LETI/DTS –CEA/GRE

9:00am 7.4 Nonuniformity of commercial SOI wafers manifested by photoluminescence and lifetime mapping

Z.Q. Li[1], M. Tajima[1], S. Sumie[2], H. Hashizume[2], A. Ogura[3]; [1]Institute of Space and Astronautical Science, [2]Kobelco Research Institute, [3]NEC Corp.

9:20am 7.5 Strain evaluation for thin strained-Si on SGOI and strained-Si on nothing (SSON) structures using nano-beam electron diffraction (NBD)

Koji Usuda, T. Numata, T. Tezuka, N. Sugiyama, Y. Moriyama, S. Nakaharai, S. Takagi; MIRAI Project, ASET

9:40am 7.6 Nano-uniformity control in Unibond® process

C. Maleville, E. Neyret, Nadia Ben Mohamed, Corinne Maunand-Tussot, Daniel Delprat; SOITEC S.A.

SESSION 8 **DEVICE DESIGN AND CHARACTERIZATION**

Chairs:Toshiro Hiramoto, Jean-Pierre Colinge

10:20am 8.1 Requirements for ultra-thin-film devices and new materials on CMOS roadmap

C. Fenouillet-Beranger[2], T. Skotnicki[1], S. Monfray[1], N. Carriere[2], F. Boeuf[1]; [1]ST Microelectronics, [2]CEA LETI

10:40am 8.2 A detailed analysis of SOI MOSFETs for SOC Design

Sushant S. Suryagandh, Mayank Garg, Jason C.S. Woo; University of California, Los Angeles

11:00am 8.3 Low Frequency Noise (LFN) characteristics of SiGe channel SOI dynamic threshold MOSFETs (SiGe-SOI-DTMOS) for low-power applications

A. Inoue, A. Asai, Y. Kawashima, H. Sorada, Y. Kanzawa, T. Kawashima, H. Hara, T. Takagi; Matsushita Electric Industrial Co., Ltd.

11:20am 8.4 Impact of non-vertical sidewall on sub-50nm FinFET

Xusheng Wu, Philip C.H. Chan, Mansun Chan; Hong Kong University of Science and Technology

11:40am 8.5 Mobility enhancement via volume inversion in double-gate MOSFETs

Lixin Ge[1], Jerry G. Fossum[2], Francisco Gámiz[3]; [1]Motorola, Inc., [2]University of Florida, [3]Universidad de Granada

12:00pm 8.6 Non-classical CMOS device design

V.P. Trivedi[1], J.G. Fossum[1], A. Vandooren[2]; [1]University of Florida, [2]Motorola, Inc.

SESSION 9 **SOI DEVICE EFFECTS AND CIRCUIT IMPACT**

Chairs: Olivier Faynot, Dimitris Ioannou

1:20pm 9.1 Impact of self-heating on digital SOI and strained-silicon CMOS circuits

K.A. Jenkins, R.L. Franch; IBM T.J. Watson Research Center

1:40pm 9.2 The impact of STI mechanical stress on the device performance of 90nm technology node with different substrates and isolation processes

Y. Jeon, G.C.F. Yeap, P. Grudowski, T. Van Gompel, J. Schmidt, M. Hall, B. Melnick, M. Mendicino, S. Venkatesan; Motorola Inc.

2:00pm 9.3 Impact ionization and band-to-band tunneling in ultrathin body SOI devices with undoped channels

R.J. Luyken, J. Hartwich, M. Specht, L. Dreeskornfeld, M. Städele, W. Rösner, F. Hofmann, E. Landgraf, T. Schulz, J. Kretz, L. Risch; Infineon Technologies

2:20pm 9.4 Anomalous history behavior in stacked PD SOI Gates

*Mark B. Ketchen[1], Manjul Bhushan[2]; [1]IBM Research, [2]IBM ISG Divisio*n

2:40pm 9.5 A new and fast method to compute steady state in PD-SOI circuits and its application to standard cells library characterization

V. Liot, P. Flatresse; ST Microelectronics

3:00pm 9.6 The role of dynamic threshold shifts in the performance of inverters and NAND gates in PD SOI technology

Mark B. Ketchen; IBM Research

SESSION 10 **LATE NEWS**

Chair: Mike Liu

ADDITIONAL INFORMATION AND AGENDA

● LATE NEWS PAPERS

Submission for the Late News Session will be accepted until August 8, 2003. Presentation of selected late papers will be on Thursday afternoon. Late News papers are not eligible for the Best Paper Award.

● POSTER SESSION

Authors will be available for questions Tuesday, September 30, 2003, 3:40pm to 5:30pm. Posters will be on display from Tuesday, 3:40pm until Thursday, 12:00pm.

● RUMP SESSION

SOI Based Systems On Chip

The Silicon On Insulator (SOI) substrate seems to be an ideal platform for System On Chip (SOC) applications as it can easily integrate various devices that might not be that compatible on bulk silicon. For example High and Low voltage devices, MEMS, high density memories and logic, high performance and low power circuits, as well as RF devices. In this rump session, world known experts in these various technologies and applications will discuss first the pros and cons of SOI as an ideal SOC substrate. Then the audience will have an opportunity to challenge the experts, propose different views to open a real debate. Will SOISOC become the future acronym in the semiconductor community? Please attend the rump session to have the answer.

● VENDOR EXHIBITS

Tuesday	3:40pm – 7:00pm (includes pre-dinner reception)
Wednesday	8:00am – 12:00pm
Thursday	8:00am – 12:00pm

Confirmed exhibitors as of July 15th:

Canon, USA, Inc
Epion Corporation
SOITEC SA

SOCIAL FUNCTIONS AND ACTIVITIES

● WELCOME RECEPTION, Monday, 6:00pm

Please join us for the kick-off event of the conference. We have planned an evening of good snacks, good drinks, and good company - all we need is you to make it complete!

● CONFERENCE BANQUET, Tuesday, 7:00pm

"Red Rover Goes to Mars: Engaging the Public in Mars Exploration" is the subject of this year's banquet speaker, Dr. Bruce Betts. Dr. Betts is the Director of Projects of the Planetary Society, a non-profit, non-governmental membership organization that supports and advocates exploration of the solar system and the search for extraterrestrial life.

● COOKOUT, Wednesday, 6:30pm

Combine great food and great networking with the great outdoors, and you have the conference "cookout" – a casual dinner under beautiful Southern California evening skies in the hotel's "Rose Garden." A great way to prepare for the Rump Session to follow!

● WEDNESDAY AFTERNOON ACTIVITIES

Newport Bay Ecological Reserve & Nature Preserve Tour

Newport Bay is home to nearly 200 species of birds, seven of which are classified as rare or endangered. The bay's waters team with over 70 species of fish, while 18 species of mammals utilize the Upper Newport Bay's habitat. The Bay was sculpted and carved by rivers during the glacial period of the Pleistocene Epoch and fossils of mammoths, bison and giant sloths have been discovered in the sedimentary deposits. The cultural history of the area spans nearly 9,000 years beginning with the Tongva Native Americans until the Spanish mission period and the coming of other settlers using the area to graze cattle and sheep. The Upper Newport Bay Ecological Reserve was dedicated in 1975 to preserve and enhance a saltwater marsh ecosystem and the various forms of life dependent upon this habitat.

Our tour will start with a visit to the Preserve's educational facility for hands on displays and a short movie about the Bay's plant and animal life. Afterwards, our guided tour will explore the mysteries of the Bay firsthand.

NEWPORT BEACH AND VICINITY

In addition to the conference's guided tour of the Newport Bay Ecological Reserve & Nature Preserve (see tour info), there are several ways to spend your "Wednesday afternoon off." The hotel offers eight lighted tennis courts and a staff of tennis pros available for lessons. There are also several challenging golf courses nearby as well as miles of jogging trails. And if this is just too much activity for you, across the street from the hotel is Fashion Island, a first-class outdoor shopping mall including Neiman Marcus and a full range of unique shops & stores that can meet the desires of every shopper.

● **AREA**: Newport Beach, California, also known as the Colorful Coast, is a sophisticated resort destination that stretches more than six miles along the scenic Pacific Ocean coastline. One of Southern California's most vibrant recreation and entertainment centers, Newport Beach is famous worldwide for its picturesque sandy beaches, majestic coastline, year-round Mediterranean climate, infinite recreational activities, award-winning dining, and world-class shopping. The world-renowned Fashion Island shopping center is just across the street from our conference hotel and California's most famous island, historic Catalina, lies only 26 miles offshore. If this is not enough, there is golfing, water sports of all sorts, and nearby Disneyland. There's more to do than you can possibly accomplish in one visit.

For more information on Newport Beach and what it has to offer, visit the Convention and Visitors Bureau online at www.newportbeach-cvb.com and request a Visitor's Guide. If you have specific needs, you can also reach the Newport Beach CVB via e-mail: info@nbcvb.com or call toll free: (800) 942-6278. If you would like to write to them, their address is:

Newport Beach CVB
3300 W. Pacific Coast Hwy., Newport Beach, CA 92663

● **WEATHER:** Expect cool to warm days between 60 - 80 degrees with cool nights. October makes for changeable weather even in California, so be prepared with warm weather clothing as well as a good jacket or coat. Dressing in layers is a good way to always be prepared for any temperature, even cool hotel rooms.

HOTEL SERVICES AND POLICIES

The conference hotel is the NEWPORT BEACH MARRIOTT HOTEL & TENNIS CLUB, 900 Newport Center Drive, Newport Beach, CA 92660. To make a reservation, please call (800) 228-9290, or fax (949) 640-4918. Be sure to say you are with the IEEE International SOI Conference to get our group rate. You can also access the hotel's website at www.marriotthotels.com/laxnb. Our group online code is IEEIEEA.

Overlooking the harbor and beyond to the ocean, the hotel boasts an accommodating location only 10 minutes from the John Wayne airport. The tennis club offers eight lighted courts with a staff of tennis pros available for lessons. There are many nearby golf courses, side trips to Disneyland, Knott's Berry Park, or Catalina Island are available. Or just relax in the whirlpool or take a refreshing swim in the pool.

● **HOTEL POLICIES & RESERVATIONS**: The Newport Beach Marriott Hotel & Tennis Club has discounted room rates for conference attendees of $129 single or double occupancy. Rooms should be reserved as soon as possible to ensure availability at the discounted rate. This special rate is available for three (3) days prior to the conference and three (3) days after the conference should you choose to extend your stay. To ensure availability, rooms should be reserved no later than September 7, 2003. A limited number of rooms are available at the prevailing Government rate to qualified attendees.

Reservations can be made by calling the hotel reservation service at (800) 228-9290 or to the hotel directly at (949) 640-4000. You may also fax the hotel reservation form to (949) 640-4055.

If you use the website www.marriotthotels.com/laxnb, use the group code: IEEIEEA to get the group rate. When making your reservations by telephone, please remember to identify yourself as an IEEE conference attendee. Check in time is 4:00pm and check out time is 12:00 noon.

A deposit must accompany all reservations in order to confirm the reservation. The deposit may be made by check, money order, or credit card. The deposit will be applied to the first night of your stay. The deposit is refundable only if notice of cancellation is received by 6:00pm the day of the reservation.

AREA AIRPORTS AND CARRIERS

● **THE NEAREST AIRPORT** serving Newport Beach is John Wayne Airport - Orange County (www.ocair.com). It is 10 minutes from the Newport Beach Marriott Hotel and the hotel provides complimentary shuttle service. Carriers at John Wayne include Alaska, Alpha Air, America West, American, Continental, Delta, Northwest, Sky West, Southwest, United, U.S. Air and Wings West.

● **INTERNATIONAL TRAVELERS PLEASE NOTE:** Few international flights fly direct to John Wayne Airport and it is likely you will need to take a connecting flight from LAX or another international airport. Please remember to allow plenty of time between flights due to ever changing security procedures in American airports.

Also, immigration rules are changing. To avoid potential problems entering the United States, it is highly recommended that you check the immigration rules that pertain to your country as soon as possible.

● **OTHER AREA AIRPORTS**

Los Angeles International Airport - (www.lawa.org) is serviced by all the major air carriers. LAX is approximately 44 miles from Newport Beach and you can expect an average driving time of one hour to the hotel, longer if arrival is during peak rush hours. Ground transportation is plentiful and includes regularly scheduled airport bus service, taxi, rental cars, and shuttle vans.

Long Beach Airport - (www.lgb.org) is serviced by American, America West, JetBlue and Horizon. Ground transportation includes taxi, rental cars, and shuttle vans. The Long Beach Airport is approximately 26 miles from Newport Beach and driving time to the hotel is approximately 40 minutes.

Ontario International Airport - (www.lawa.org) is serviced by Alaska, America West, American, American Eagle, Continental, Frontier. JetBlue, Northwest, Southwest, United and U.S. Air Express. Ontario is approximately 46 miles from Newport Beach and driving time to the hotel is approximately 70 minutes. Ground transportation includes taxi, rental cars, and shuttle vans.

AIRPORT SHUTTLES RENTAL CARS RAIL SERVICES

The cost of ground transportation will vary depending upon the type of transportation and the distance to the hotel.

● **Arriving from John Wayne Airport:** The Newport Beach Marriott Hotel & Tennis Club offer complimentary shuttle service between the hotel and John Wayne Airport–Orange County. The daily shuttle departs the hotel for the airport approximately every 30 minutes from 7:00am through 10:30pm.

● **Arriving from Los Angeles International Airport**: Ground transportation to the hotel includes regularly scheduled airport bus service, taxis, rental cars, and shuttle vans, but the trip to Newport Beach can easily take more than an hour.

● **Rental Car Phone Numbers**:

Alamo	(800) 327-9633	Hertz	(800) 654-3131
Avis	(800) 331-1212	National	(800) 227-7368
Budget	(800) 527-7000	Thrifty	(800) 847-4389

● **Hotel Parking:** Self-Parking at $1.00 per hour to a maximum of $10.00 per day or $9.00 for overnight guests. Valet parking is available at $12.00 overnight with unlimited entries and exits.

● **BY RAIL**

If you would like to take the scenic route without having to drive, call Amtrak for information and reservations at (800) 872-7245. Amtrak's web site is www.amtrak.com. Click on "reservations" to purchase tickets in advance. If you check out the "Rail Sale" selection, you will find the latest special rates.

There are two rail stations near the Newport Beach Marriott Hotel. Both stations have taxis available to transport you to the hotel. Taxi fees will vary.

Santa Ana Station	1000 E. Santa Ana Blvd., Santa Ana, CA 92701 (714) 547-8389 13 miles (approx. 16 minutes) from the hotel
Irvine Station	15215 Barranca Pkwy., Irvine CA 92618-2214 12 miles (approx. 17 minutes) from the hotel

DRIVING DIRECTIONS

Please be aware that Southern California traffic changes dramatically depending on the time of day you are driving. Heavy traffic can be expected 7am to 9am and 4pm to 7pm. in most areas. Although part of the drive includes the San Joaquin Toll Road only travelers taking the toll road from San Diego will pass through a toll gate and must pay a toll. There is no toll gate, and therefore no toll, the north end of the toll road to Newport Beach. If you do plan to use the San Joaquin Toll Road to travel from the San Diego area, we recommend bringing at least $5 in quarters to make your trip easier.

Self-parking at the Newport Beach Marriott is $1.00 per hour to a maximum of $10.00 per day or $9.00 for overnight guests. Valet parking is available at $12.00 for overnight guests with unlimited entries and exits.

● **From Los Angeles International Airport** - Take the San Diego Freeway (405) south to San Joaquin Hills Toll Road (73). Exit on Jamboree Road, turning right toward Corona del Mar. Continue down Jamboree Road to Santa Barbara Drive. Turn left on Santa Barbara Drive. The hotel will be on the right at the top of the hill.

● **From John Wayne Airport** - Take MacArthur south to Jamboree Road. Turn right on Jamboree Road. Continue down Jamboree to Santa Barbara Drive. Turn left on Santa Barbara Drive. The hotel will be on the right at the top of the hill.

● **From Long Beach Airport** - Take the San Diego Freeway (405) south to San Joaquin Hills Toll Road (73). Exit on Jamboree, turning right toward Corona del Mar. Continue down Jamboree Road to Santa Barbara Drive. Turn left on Santa Barbara Drive. The hotel will be on the right at the top of the hill.

● **From Ontario International Airport** - Take the San Bernardino Freeway (10) west to the Orange Freeway (57) south to the Santa Ana Freeway (5) south to the Newport Freeway (55) south to the San Joaquin Hills Toll Road (73). Exit on Jamboree, turning right toward Corona del Mar. Continue down Jamboree Road to Santa Barbara Drive. Turn left on Santa Barbara Drive. The hotel will be on the right at the top of the hill.

If you are unsure of these directions, please check one of the Internet's many mapping services for additional information.

CONFERENCE REGISTRATION

● **ON-SITE CONFERENCE REGISTRATION SCHEDULE**

Sunday, September 28	6:00pm - 8:00pm
Monday, September 29	7:00am - 5:00pm
Tuesday, September 30	7:00am - 5:00pm
Wednesday, October 1	7:00am - noon
Thursday, October 2	7:00am - noon

● **TO REGISTER**

- Use the enclosed registration form or download a PDF form from our web site.
- Complete the registration form. Please fill-in all information completely.
- Mail or fax your registration form and payment no later than September 8, 2003 to:

IEEE International SOI Conference
520 Washington Blvd., #350
Marina del Rey, CA 90292 USA
310/305-1038

- Telephone registration is not available
- Do not send your hotel reservation form with the conference registration form; send the hotel reservation form to the hotel.
- Please remember to include payment with your mailed or faxed form as only forms accompanied by payment will be accepted. There are no exceptions. You may pay for your registration with either a check or a credit card.
- If you cannot mail or fax your form and your payment by September 8, 2003, you must register on-site at the conference (see On-site Registration Schedule).

● **TO PAY BY CREDIT CARD**

Complete the registration form including the Credit Card Information section and either fax it to 310/305-1038 or mail it to 2003 IEEE International SOI Conference, c/o BACM, 520 Washington Blvd., #350, Marina del Rey, CA 90292. Please be sure that the credit card information is complete, legible, and includes your signature.

● TO PAY BY CHECK

Complete the registration form and mail it with your check to 2003 IEEE International SOI Conference, c/o BACM, 520 Washington Blvd., #350, Marina del Rey, CA 90292. Please make checks payable to 2003 IEEE SOI Conference. All checks must be drawn on a US bank and in US funds only.

● CANCELLATIONS

Cancellation requests must be made in writing to the conference manager. Refund requests received by Monday, September 15, 2003 will receive a refund of registration fees paid less a $25 processing fee. Requests received after September 15, 2003 will be considered by the committee. All refunds will be processed after the conference.

● INCLUDED MEALS

Short Course/Tutorial:

Continental breakfast & lunch on Monday

Conference:

Monday - Welcome Reception

Tuesday - Continental breakfast & dinner with reception

Wednesday - Continental breakfast & "Cook-Out" dinner

Thursday - Continental breakfast

Please note: You are on your own for lunch Tuesday, Wednesday, and Thursday, as well as for dinner on Monday.

ADDITIONAL INFORMATION

For additional conference and registration information please contact:

BACM
520 Washington Blvd., #350
Marina del Rey, CA 90292
Tel: 310.305.7885 ?Fax: 310.305.1038
e-mail: bacm@attbi.com

KEY TELEPHONE NUMBERS

Conference Manager

Tel: 310.305.7885 • Fax: 310.305.1038

Newport Beach Marriott

Tel: 800.228.9290 • Fax: (949) 640-4918
website: www.marriott.com/laxnb
Click on "Reserve a Room" - the group code is IEEIEEA

Newport Beach Visitor's Bureau

Tel: 800.942.6278
www.newportbeach-cvb.com