GENERAL CHAIR'S GREETING

On behalf of the conference committee, I am pleased to invite you to the 2004 IEEE International Silicon on Insulator (SOI) Conference. As with previous conferences, the 2004 SOI Conference continues to provide a forum for the interaction of scientists and engineers interested in all aspects of SOI technologies. This year we have selected an outstanding Technical Program and a particularly hot topic for the one-day Short Course to begin the conference.

The Technical Program Committee, chaired by Dr. James Burns of MIT Lincoln Labs, has worked hard to select an exceptional set of papers this year that substantially advance the field. These contributions should broaden the perspective of the active specialists with new information and provide the necessary background for the newcomers in the field. Three invited speakers will lead off the conference in the plenary session on Tuesday discussing SOI applications and technology and their future.

This year's Short Course is, "NOVEL DEVICES ON SOI." It will be delivered by four specialists covering the following areas critical in building novel devices: SOI Substrates, Transistor Options, Integration and Manufacturing Challenges, and Modeling and Simulation. The short course is organized by Dr. Pierre Fazan of the LEG Laboratory, Swiss Federal Institute of Technology. It will be presented Monday, October 4th

The panel discussion will take place Wednesday evening after the cookout. This year's topic, "READINESS OF DOUBLE-GATE TRANSISTORS: IS THERE A WINDOW FOR UT/FD SOI?," is organized by Dr. Mario M. Pallela of Advanced Micro Devices. The panel of distinguished experts will discuss their views on technology, material, scalability, and performance related to this controversial area.

The friendly and informal atmosphere that contributes to the success of our conference year after year is enhanced by a number of social events for attendees and their guests. Our social program begins with a welcome reception on Monday evening October 4th. On Tuesday night, after the poster session, the conference banquet will take place. Dr. Fred Bernache of Freescale Semiconductor, Transportation and Standard Products Group will be the speaker. He will discuss the substantial technology infusion in automotive electronics and what it means to the consumer in the coming years.

Finally, I would like to express my sincere thanks to all the authors and participants for making the conference successful. I would also like to acknowledge the hard work and dedication of the executive and technical committees as well as the conference management team for pulling together this excellent program.

Sincerely,
Michael Mendicino, General Chair

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30TH ANNUAL IEEE INTERNATIONAL SOI CONFERENCE

EXECUTIVE COMMITTEE

GENERAL CHAIR
Michael Mendicino, Motorola
Tel: 512.933-7283 • Fax: 512.933-5304
Email: RA1458@email.sps.mot.com

Mike Mendicino received his BS degree from Ohio State University in 1989, and his MS and PhD degrees in chemical engineering from the University of Illinois in 1994. He completed a two-year assignment at SEMATECH where he was a project leader responsible for thin film SOI materials characterization and development. He is currently with Motorola's Digital DNA Laboratories working on advanced device technologies for high performance CMOS applications. Mike is a fellow of the technical staff at Motorola and member of IEEE.

LOCAL ARRANGEMENTS CHAIR
Christophe Tretz, IBM–San Jose Design Center
408/888-3852 • ctretz@us.ibm.com

Dr. Christophe Tretz received his BSc degree (1991) from the Ecole Nationale Superieure d'Electronique, Electrotechnique, Informatique et Hydraulique de Toulouse (ENSEEIHT), France, and his MS (1992) and PhD in electrical engineering (1997) from Columbia University, New York. He joined IBM at the TJ Watson Research Center in Yorktown Heights, NY in 1997 and contributed to the design of several microprocessors for servers and workstations both with bulk and SOI processes. In 2000, he joined Advanced Micro Devices, in the California Microprocessor Division, as a member of the technical staff, where he was contributing to the design of the Hammer microprocessor family and establishing design guidelines for microprocessor using SOI technologies. He is now back with IBM as a senior circuit design engineer in the San Jose Design Center for the Engineering and Technology Services Division. Dr. Tretz has authored or co-authored about 20 papers and three US patents in the field of circuit design techniques using SOI, circuit optimization, and low power design. His current research interests remain in optimizing circuit design for SOI and in improving design choices for SOI.

TECHNICAL PROGRAM CHAIR
James Burns
MIT Lincoln Laboratory, Advanced Silicon Technology
781/981-2654 • jab@ll.mit.edu

James A. Burns received his BS degree in physics from the Carnegie Institute of Technology in 1960 and his PhD degree in physics from the University of Vermont in 1975. He worked in semiconductor and magnetic film device design and processing at IBM and CCD design while at Honeywell. Since 1975 he has been a staff member at MIT's Lincoln Laboratory where his principal interests are silicon transistor and process design and the development of analytical techniques to customize IC fabrication to integrated circuit applications. He developed the laboratory's deep sub-micron fully depleted SOI process and is currently working on integrating that SOI technology into a three-dimensional integrated circuit technology. He is a member of the American Physical Society, IEEE, and Tau Beta Pi.

TREASURER AND REGISTRATION CHAIR
Toshiro Hiramoto, University of Tokyo,
Institute of Industrial Science
Tel: 81 3 5452-6263 • hiramoto@nano.iis.u-tokyo.ac.jp

Toshiro Hiramoto received his BS, MS, and PhD degrees in electronic engineering from the University of Tokyo in 1984, 1986, and 1989, respectively. In 1989, he joined Device Development Center, Hitachi Ltd., Ome, Japan, where he was engaged in the device and circuit design of ultra-fast BiCMOS SRAMs. In 1994, he joined the Institute of Industrial Science, University of Tokyo, Japan, as an associate professor. He was also an associate professor at VLSI Design and Education Center, University of Tokyo, from 1996 to 2002. He has been a professor at the Institute of Industrial Science, University of Tokyo since 2002. His research interests include low power and low voltage design of advanced CMOS devices, SOI MOSFETs, device/circuit cooperation scheme for low power VLSI, quantum effects in nano-scale MOSFETs, and silicon single electron transistors. Dr. Hiramoto is a member of IEEE, IEICE, and Japan Society of Applied Physics. He has been an Elected AdCom Member of IEEE Electron Devices Society since 2001. He served as the program chair of Silicon Nanoelectronics Workshop in 1997, 1999, and 2001, and as the general chair of Silicon Nanoelectronics Workshop in 2003.

SENIOR CONFERENCE COMMITTEE

RUMP AND POSTER CHAIR
Mario M. Pelella, Advanced Micro Devices
(408)749-4321 • mario.pelella@amd.com

Mario M. Pelella (S'81, M'85, SM'04) received his BS and MS degrees in electrical engineering from Clarkson University, Potsdam, NY, in 1983 and 1985, respectively. He received his PhD degree in electrical and computer engineering at the University of Florida, Gainesville in 2000. He joined IBM Microelectronics (General Technology) Division in 1985 where he worked on the device design and modeling of advanced high-speed bipolar transistor technologies and more recently engaged on advanced Silicon-on-Insulator (SOI) CMOS technologies for IBM's, DARPA's and NCCOSC's Low Power Electronics programs. In 1996 he joined the Silicon Technology Innovation and Modeling group at the IBM TJ Watson Research Center, Yorktown Heigths, NY where he worked on improvements to TCAD modeling tools and the analysis of floating-body effects in scaled PD/SOI technologies. He joined the logic technology development group at Advanced Micro Devices in 2000 where he is currently engaged in the development of scaled SOI technologies for the next generation of microprocessors. His research and development interests continue to include the device design, modeling and performance analysis of advanced SOI CMOS technologies, as well as Electrostatic Discharge (ESD) protection devices. He has received over 15 US patents and is an author of over 40-refereed publications. Dr. Pelella was chairman of the IEEE Electron Device Society Mid Hudson Valley Chapter, 1995-1997, participated on the 1995-1996 and 1996-1997 National Technology Roadmap Committee for Semiconductor Compact Modeling, served on the IEEE International SOI Conference technical program committee during 1996-1998 and is now serving on the 2004 senior committee. He was the recipient of the Semiconductor Research Corporation (SRC) outstanding industrial mentor award in 1996. He received a 1983, 1984 TI Fellowship award and a 1998, 1999 IBM Cooperative Fellowship award to pursue his academic research and he was elected senior member of the IEEE in 2004.

SHORT COURSE CHAIR
Pierre Fazan, LEG Laboratory,
Swiss Federal Institute of Technology
+41-21-6934604 • pierre.fazan@epfl.ch

Pierre C. Fazan was born in Lausanne, Switzerland where he obtained his physics diploma and PhD degrees at the Swiss Federal Institute of Technology (EPFL) in 1984 and 1988 respectively. From 1989 to 1997 he worked as process integration engineer then manager at Micron Technology, Boise USA, focusing on DRAM process integration. In 1997 he was named Professor at the Swiss Federal Institute of Technology, Lausanne, EPFL, where he teaches in the field of IC manufacturing. In 1999 he founded Innovative Silicon Solutions, a consulting company specialized in embedded memory design and integration. In 2002 he co-founded Innovative Silicon, an IP startup developing a new SOI single transistor memory concept. This company was funded in December 2003. He authored or co-authored more than 100 papers and invented or co-invented more than 150 US patents. Dr. Fazan has served as member in program committees of the SOI Conference, IEDM, VLSI Tech. Symp, ISIF, ESSDERC, INFOS and ECS Conferences.

❖❖ TECHNICAL COMMITTEE ❖❖

Richard Brown, *University of Utah*
Jean-Pierre Colinge, *UC Davis*
Paul Fechner, *Honeywell SSEC*
Samuel Fung, *Taiwan Semiconductor Mfg.*
Keith Jenkins, *IBM/TJ Watson Research*
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❖❖ ADVISORY COMMITTEE❖❖

Theodore Houston,*Texas Instruments*
Harry Hovel, *IBM Corporation*
Dimitris Ioannou, *George Mason University*
Michael Liu, *Honeywell SSEC*

SHORT COURSE OVERVIEW & AGENDA

The SOI short course was initiated in 1995 with the staged goal of providing a general background about prior work in the field as well as a general overview of future technical issues and directions.

The theme of this year's short course is "Novel Devices on SOI." The size of MOS devices continues to shrink according to Moore's law. The ITRS predicts that this scaling will continue to few nm gate length devices over the next 15 years and that it will face serious technical challenges. Recently well publicized issues mention excessive power consumption of logic circuits due to various leakages, performance saturation or the lack of dense embedded memories. To address those issues and continue full steam ahead, the semiconductor industry is introducing SOI devices. Those appear first as simple planar devices such as Partially Depleted (PD) or Fully Depleted (FD) transistors. Then they migrate to more complex planar or 3 dimensional (3D) structures such as double gate, vertical gates, FinFET, or various flavors of multi gate devices. New engineered substrates are also introduced to boost performance. The objective of this course is to give the attendees a basic idea of these trends and features.

In the first presentation, a special focus is put on the basic materials or substrates on which those devices are integrated. Dr. C. Maleville and Dr. I Cayrefourcq of Soitec will introduce the various substrates that are considered to sustain Moore's law. This will cover SOI materials, strained materials as well as GeOI. Specific metrology required will be described and a substrate roadmap will be presented.

In the second tutorial, the various transistor options proposed for present and future applications are reviewed by Dr. S.F. Huang of IBM. This will include PD SOI, FD SOI, strained Si on SOI, double gate and FinFET 3D devices. These various devices structures and operation principles will be described.

Then integration and manufacturing challenges are considered to assess the complexity and manufacturability of all considered options. This topic will be covered by Dr. K. DeMeyer from IMEC who will first cover regular planar SOI devices and then move to multi gate devices, including planar double gate, SON, FinFET as well as more futuristic devices.

Finally, the modeling and simulation of these devices and their numerous evolutions are reviewed critically by Dr. A. Schenk of ETHZ. This tutorial will consider quantum mechanical confinement effects, tunnel generation in the drain-body junction (GIDL, trap assisted tunneling), gate tunneling, source to drain tunneling and quantum ballistic effects and a final outlook on the future simulation challenges.

❖❖ SHORT COURSE AGENDA❖❖

7:00am - 5:00pm	Registration
7:00am - 8:00am	Continental Breakfast
8:30am - 9:00am	**Introduction,** *P. Fazan, EPFL*
9:00am - 10:00am	**SOI Substrates & Substrates Engineering** *C. Maleville, Soitec,* *I. Cayrefourcq, Soitec*
10:00am - 10:15am	Break
10:15am - 11:45am	**SOI Transistor Options** *S.F. Huang, IBM*
12:00pm - 1:30pm	Hosted Lunch
1:30pm - 3:00pm	**Process Integration & Manufacturing Challenges** *K. De Meyer, IMEC*
3:00pm - 3:15pm	Break
3:15pm - 4:45pm	**Modeling & Simulation of SOI Devices** *A. Schenk, ETHZ*
4:45pm - 5:00pm	Course Wrap-up
6:00pm - 8:00pm	Welcome Reception

SHORT COURSE INSTRUCTORS

Christophe Maleville • Dr. Maleville is process engineering manager at Soitec (Bernin, France). Since 1993 he has been involved with the development of the Smart Cut process in collaboration with Commissariat à l'Energie Atomique/Laboratoire d'Electronique de Technologie d'Information (CEA/LETI) and has worked on its application to the manufacturing of SOI wafers. Currently he participates in new SOI process development and in transferring SOI technology to production. He has authored or co-authored more than 30 papers dealing with SOI manufacturing and metrology and holds approximately 15 patents in that area. He received a PhD in microelectronics from the Institut Polytechnique de Grenoble.

Ian Cayrefourcq • Dr. Cayrefourcq joined Soitec in 2002, where he is currently the New Technology Development Department manager. Previously, he worked four years at Thales as R&D engineer in optoelectronics. Then, in 1998, he joined Corning Inc. as project leader in charge of developing Dynamic Gain Flattening Filters. He received an engineering degree in material science, a master's degree in solid state physics and a PhD in microelectronics from IEMN (Institute of Electronics and Microelectronics of northern France). He owns more than ten patents and authored or co-authored more than 20 publications relative to SOI.

Shih-Fen Huang • Dr. Huang received her BS and MS degrees from National Taiwan University, in 1989 and 1991, respectively, and her PhD degree from Stanford University in 1998. From 1992 to 1997, she was a graduate student researcher in the Center for Integrated Systems at Stanford University. From 1997 to 1999, she was a senior engineer in LSI Logic, Santa Clara, CA. She joined IBM Semiconductor Research and Development Center, as a development staff member in 1999, where she worked on development of DRAM and high performance CMOS logic. She is currently Senior Manager of high performance SOI logic device design. She holds three US patents, and has 12 US patent applications pending.

Kristin De Meyer • Dr. De Meyer received her degree in electrical engineering in 1974 and her PhD degree in 1979, both from the Katholieke Universiteit Leuven (KUL). From November 1979 through November 1980 she was granted an IBM World Trade Post Doctoral Fellowship and worked at the IBM Thomas J. Watson Research Centre, Yorktown Heights on the development of EAROMs using Si-rich oxides. At the end of 1980 she returned to the KUL as a senior research assistant of the NFWO, and from October 1982 as a research associate of the NFWO. With the foundation of IMEC, her activities moved from the KUL to IMEC, where she initially remained research associate of the NFWO. Since October 1989 she is a regular employee of IMEC. From 1985 through 1992 she was in IMEC head of the group on Process and Device Modeling and Simulation. Also Statistical Process Control Activities (SPC) were monitored through her group. From January 1993 through December 2002 she was in charge of deep submicron MOS technology and exploratory field effect devices. From January 2003 she became Strategic Coordinator of Doctoral Research in IMEC. Since October 1986 she is also a part-time professor at the KUL. She authored or co-authored over 200 publications and organized summer courses, the SISPAD 98 conference and the ULIS 2004 workshop.

Andreas Schenk • Dr. Schenk received his Dipl. Phys. degree and his PhD from Humboldt University in Berlin (HUB) in 1981 and 1987, respectively. From 1987 until 1991 he worked on various aspects of the physics and simulation of optoelectronic devices. In 1991 he joined the Integrated Systems Laboratory (ISL) of ETH working as a senior research/teaching assistant, where he qualified to give lectures at university in 1997 for "Physics and Modeling of Microelectronic Devices." His main activities are in the physics-based modeling for advanced simulation of submicron silicon devices and their application in the TCAD software released by ISE AG Zurich. These models include many-body effects, generation-recombination, mobility, contacts, heterojunctions, single electron transistor modeling at device level, and quantum effects in silicon ultra-small devices with emphasis on barrier tunneling, resonant tunneling, scattering rates, and currents. He is head of the device physics group at ISL. He authored and co-authored two books and 100 papers.

PROGRAM SCHEDULE AT-A-GLANCE

REGISTRATION	Sunday, October 3	6:00pm - 8:00pm
	Monday, October 4	7:00am - 5:00pm
	Tuesday, October 5	7:00am - 5:00pm
	Wednesday, October 6	7:00am - 12:00pm
	Thursday, October 7	7:00am - 12:00pm
EXHIBITS OPEN	Tuesday, October 5	3:40pm - 7:00pm
	Wednesday, October 6	8:00am - 12:00pm
	Thursday, October 7	8:00am - 12:00pm

CONFERENCE SCHEDULE

MONDAY, October 4th

7:00am	Short Course Breakfast
8:30am	Short Course
12:00pm	Short Course Lunch
1:30pm	Shout Course
6:00pm	Welcome Reception

TUESDAY, October 5th

7:00am	Continental Breakfast
8:00am	Introduction & Welcome
8:15am	**Session 1:** PLENARY SESSION
10:15pm	Break
10:30am	**Session 2:** DEVICES
12:30pm	Lunch
1:30pm	**Session 3:** SOI MATERIALS AND PROCESS TECHNIQUES
3:30pm	**Session 4:** POSTER SESSION
6:30pm	Banquet Reception
7:00pm	Banquet

WEDNESDAY, October 6th

7:00am	Continental Breakfast
8:00am	Session 5: CIRCUIT TECHNIQUES AND APPLICATIONS
10:00am	Break
10:20am	Session 6: NOVEL MATERIALS, PROCESSES, AND DEVICES
12:20pm	Lunch & Activities
6:30pm	Cookout Dinner
8:00pm	Rump Session

THURSDAY, October 7th

7:00am	Continental Breakfast
8:00am	**Session 7:** DEVICE CHARACTERIZATION, MODELING AND SIMULATION
10:00am	Break
10:20am	**Session 8:** ANALOG, MIXED MODE, AND RF
12:20pm	Lunch
1:20pm	**Session 9:** DEVICES - DOUBLE GATE
3:20pm	Break
3:40pm	**Session 10:** LATE NEWS
5:40pm	Wrap-up & Presentation of Best Paper Award

THE TECHNICAL PROGRAM *will consist of 42 oral and 19 poster papers, as well as three invited talks. Technical Sessions and Session Chairs are as follows:*

Session 1	**PLENARY** *Chair: James Burns*
Session 2	**DEVICES** *Chairs: Keith Jenkins, Toshiro Hiramoto*
Session 3	**SOI MATERIALS AND PROCESS TECHNIQUES** *Chairs: Paul Fechner, Carlos Mazure*
Session 4	**POSTERS** *Chair:* Mario Pelella
Session 5	**CIRCUIT TECHNIQUES AND APPLICATIONS** *Chairs: Christophe Tretz, Richard Brown*
Session 6	**NOVEL MATERIALS, PROCESSES, AND DEVICES** *Chairs: Atsushi Ogura, Thierry Poiroux*
Session 7	**DEVICE CHARACTERICATION, MODELING AND SIMULATION** *Chairs: Dimitris Ioannou, Mike Liu*
Session 8	**ANALOG, MIXED MODE, AND RF** *Chairs: Ted Houston, Hector Sanchez*
Session 9	**DEVICES - DOUBLE GATE** *Chairs: J.P. Colinge, Shigeru Kawanaka*
Session 10	**LATE NEWS** *Chair: Michael Mendicino*

TECHNICAL PROGRAM SCHEDULE

Tuesday, October 5th

SESSION 1 **PLENARY SESSION**
Chair: James Burns

8:15am 1.1 SOI for Hostile Environmental Applications
Jean-Pierre Colinge, Univ. of California, Davis

8:55am 1.2 A VLSI Methodology for SOI Technology
David Allen, IBM Corporation

9:35am 1.3 The future of SOI in microlelectronic systems
Zachary Lemnios, DARPA

SESSION 2 **DEVICES**
Chairs: Keith Jenkins, Toshiro Hiramoto

10:30am 2.1 10nm-gate-length transistors on ultra-thin SOI film: process realization and design optimisation
J. Lolivier[1], M. Vinet[1], T. Poiroux[1], B. Previtali[1], T. Chevolleau[2], J.M. Hartmann[1], A.M. Papon[1], R. Truche[1], O. Faynot[1], R. Balestra[3], S. Deleonibus[3]; [1]CEA/DRT-LETI, [2]LTM/CNRS-UJF, [3]IMEP-ENSERG

10:50am 2.2 Body Voltage and History Effect Sensitivity to Key Device Parameters in 90nm PD-SOI
S. Kawanaka[1], M.B. Ketchen[2], M. Bhushan[2], D.J. Pearson[2], R. Bhasin[3], K. Mcstay[3], M.Sherony[3], P. Fisher[4], K. Matsumoto[5], H. Utomo[3], H. Nii[1], H. Harifuchi[5], G. Sudo[1], W. Rausch[3], H. Kimura[5], T. Nakao[1], H. Park[3], S.H. Oh[3], A. Waite[4], S. Womack[3], S. Narasimha[3], A.C. Mocuta[3], A. Ajmera[3], Y. Li[3], R. Malik[3], Y. Kohyama[1], J. Cheek[4], I. Yang[3], W.F. Clark[3], R. Divakaruni[3], Y. Li[3]; [1]Toshiba America Electronic Components Inc., [2]IBM T.J. Watson Research Center, [3]IBM Microelectronics SRDC, [4]AMD Corporation, [5]Sony Electronics Inc.

11:10am 2.3 Physical modelling and design of thin film SOI lateral PIN Photodiodes for Blue DVD-applications
A. Afzalian, D. Flandre; Université catholique de Louvain

11:30am 2.4 An investigation of ESD Protection Diode Options in SOI
C. Putnam, M. Woo, R. Gauthier, M. Muhammad, K. Chatty, C. Seguin, R. Halbach; IBM Microelectronics Semiconductor Research & Development Center

11:50am 2.5 Energy-Delay Optimization of Thin-Body MOSFETs for the Sub-15 nm Regime
S. Balasubramanian, J. L. Garrett, V. Vidya, B. Nikolic, T.J. King; University of California, Berkeley

12:10pm 2.6 Total Dose Radiation Effects in Partially-Depleted SOI Transistors with Ultrathin Gate Oxide
B. Jun[1], M. Fouillat[2], R.D. Schrimpf[1], D.M. Fleetwood[1], S. Cristoloveanu[3]; [1]Vanderbilt University, [2]Department of the IUT Measures Physiques Bordeaux, [3]MEP, ENSERG

Please also see Session 2 posters P2.1, P2.2, P2.3

SESSION 3 **SOI MATERIALS AND PROCESS TECHNIQUES**
Chairs: Paul Fechner, Carlos Mazure

1:30pm 3.1 Fabrication of Strained Si/Strained SiGe/ Strained Si Heterostructures on Insular by a Bond and Etch-back Technique
I. Aberg[1], O.O. Olubuyide[1], J. Li[2], R. Hull[2], J.L. Hoyt[1]; [1]MIT Microsystems Technology Laboratories, [2]University of Virginia

1:50pm 3.2 300 mm SGOI/Strain-Si for High-Performance CMOS
A. Rezincek, S.W. Bedell, H.J. Hovel, K.E. Fogel, J.A. Ott, R. Mitchell, D.K. Sadana; IBM Thomas J. Watson Reseach Center

2:10pm 3.3 Crystal-direction dependence of uniaxial strain in ultra-thin SOI
R.L. Peterson[1, 3], K.D. Hobart[2], H. Yin[1], J.C. Sturm[1]; [1]Princeton Institute for the Science and Technology of Materials (PRISM) and Department of Electrical Engineering, Princeton University, [2]Naval Research Lab

2:30pm 3.4 Influence of the mechanical strain induced by a metal gate on electron and hole transport in single and double-gate SOI MOSFETs
T. Guillaume[1], M. Mouis[1], S. Maitrejean[2], A. Poncet[3], M. Vinet[2], S. Deleonibus[2]; [1]MEP, UMR, [2]CEA/LETI, [3]LPM, UMR

2:50pm 3.5 Use of LPCVD TEOS as a direct bonding material for layer transfer: Densified vs. Undensified
G. Ilicali[1,2], W. Rösner[1], W. Weber[1,2], S. Boz[1], L. Dreeskornfeld[1],J. Hartwich[1], J. Kretz[1], J.R. Luyken[1], E. Landgraf[1], F. Hofmann[1], L. Risch[1], W. Hansch[2]; [1]InfineonTechnologies AG, [2]Technical University Munich

3:10m 3.6 Enhanced High resistivity SOI wafers for RF application
D. Lederer, R. Lobet, J.P. Raskin; Université catholique de Louvain

Please also see Session 3 posters P3.1, P3.2, P3.3

SESSION 4 POSTERS
3:30pm *Chair:* Mario Pelella

Note: Poster numbers were chosen to associate the posters by technical content with the oral session. Poster, P3.1, means the poster, P, is the first poster similar in technical content to the papers presented in session 3; P3.2 is the second poster with similar content to session 3.

P2.1 Threshold Voltage of Sub-10-nm-Thick SOI MOSFETs at Cryogenic Temperature and Quantum Effects
Y. Omura, A. Nakakubo, H. Nakatsuji; Kansai University

P2.2 Influence of a Tunneling Gate Current on the Noise performance of SOI MOSFETs
G. Paillocny[1], B. Iniguez[2], G. Dambrine[1], F. Danneville[1]; [1]IEMN CNRS UMR, [2]Universitat Rovira, [1]Virgili

P2.3 Degradation of Body Factor ((y) of Single Gate Fully Depleted SOI MOSFETs Due to Short Channel Effects
A. Kumar, T. Nagumo, G. Tsutsui, T. Hiramoto, University of Tokyo

P3.1 Fabrication of High Quality Patterned SOI Materials by Optimized Low-Dose SIMOX
Y. Dong[1,2], M. Chen[1,2], J. Chen[2], X Wang[1,2]; [1]Shanghai Simgui Technology Co., Ltd., [2]Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences

P3.2 Alternative Dielectrics for Advanced SOI MOSFETs: Thermal Properties and Short Channel effects
N. Bresson[1,2], S. Cristoloveanu[2], K. Oshima[2,3], C. Mazuré[1], F. Letertre[1], H. Iwai[3]; [1]SOITEC, S.A., [2]IMP (UMR CNRS-INPG-UJF), [3]Tokyo Institute of Technology

P3.3 Plasma-Activated Bonding, Contolled Cleave Process, and Non-Contact Smoothing for Germanium-on-Insulator (GeOI) Manufacturing
H.R. Kirk, A. Lamm, A. Paler, P.J. Ong, I.J. Malik, S. Kang, F.J. Henley; Silicon Genesis Corporation

P5.1 High Performance and Low Power Domino Logic Using Independent Gate Control in Double-Gate SOI MOSFETs
H. Mahmoodi, S. Mukhopadhyay, K. Roy; Purdue University

P5.2 Effectiveness of Using Supply Voltage as Back-Gate Bias in Ground Plane SOI MOSFETs
C.H. Kim[1], H. Ananthan[2], J.J. Kim[3], K. Roy[2]; [1]Department of ECE, University of Minnesota, [2]School ECE, Purdue University, [3]IBM TJ Watson Research Center

P6.0 An Investigation of Wafer-to-Wafer Alignment Tolerances for 3-Dimensional Integrated Circuit Fabrication
K. Warner, C. Chen, R. D'Onofrio, C. Keast, S. Poesse; Lincoln Laboratory, Massachusetts Institute of Technology

P7.1 New and Accurate Method for Electrical Extraction of Silicon Film Thickness on Fully-Depleted SOI and Double Gate Transistors
T. Poiroux[1], J. Widiez[2], J. Lolivier[1], M. Vinet[1], M. Cassé[1], B. Prévitali[1], S. Deleonibus[1]; [1]CETI-DRT-LETI-CEA/GRE, [2]STMicroelectronics

P7.2 Detailed Investigation of Geometrical Factor for Pseudo-MOS Transistor Technique
K. Komiya[1], N. Bresson[2,3], S. Sato[1], S. Cristoloveanu[2], Y. Omura[1]; [1]Kansai University, [2]MEP (UMR CNRS-INPG-UJF), [3]SOITEC Corp.

P7.3 2D Poisson-Schrodinger simulations in Ultra-Thin Silicon-on-Nothing devices: Quantum effects impact evaluation
D. Chanemougame[1], A. Poncet[2], S. Monfray[1], A. Souifi[2], H. Bourdon[2], A. Talbot[1], F. Leverd[1], D. Delille[3], T. Skotnicki[1]; [1]ST Microelectronics, [2]Laboratoire de Physique de la Matiére, [3]Philips Semiconductors

P7.4 Assessing the Performance Limits of Ultra-Thin Double-Gate MOSFETs: Silicon vs. Germanium
A. Khakifirooz, O. M. Nayfeh, D. A. Antoniadis; Microsystems Technology Laboratories, Massachusetts Institute of Technology

P7.5 Thermal Modeling of Silicon-On-Insulator Current Mirrors
F. Yu, M.C. Cheng; Clarkson University

P8.1 Impact of Buried Oxide Thickness and Ground Plane Resistivity on Substrate Cross-Talk in Ground Plane Silicon-on-Insulator (GPSOI) Cross-Talk Suppression Technology
S. Stefanou[1], J.S. Hamel[2], P. Baine[3], M. Bain[3], B.M. Armstrong[3], H.S. Gamble[3], M. Kraft[1], H.A. Kemhadjian[1]; [1]Univ. of Southampton, UK, [2]Univ. of Waterloo, Waterloo, Ontario, Canada, *[3]The Queen's University of Belfast*

P8.2 DC and RF Characterization of Fully-Depleted Strained SOI MOSFETs
C.L. Chen[1], T.A. Langdo[2], C.K. Chen[1], J.G. Fiorenza[2], P.W. Wyatt[1], M.T. Currie[2], C.W. Leitz[2], G. Braithwaite[2], Z. Cheng[2], A. Lochtefeld[2], C.K. Keast[1]; [1]Lincoln Laboratory, Massachusetts Institute of Technology, [2]AmberWave Systems Corporation

P9.1 Threshold Voltage Model of the SOI 4-Gate Transistor
K. Akarvardar, S. Cristoloveanu, P. Gentil; IMEP, ENSERG

P9.2 Characterization of Edge Direct Tunneling Leakage of Gate Misaligned Double Gate MOSFETs
C.Yin, P.C.H. Chan; Hong Kong University of Science and Technology

P9.3 Impact of Underlap on Gate Capacitance and Gate Tunneling Current in 16nm DGMOS Devices
A. Bansal, B. C. Paul, K. Roy; Purdue University

Wednesday, October 6th

SESSION 5 CIRCUIT TECHNIQUES AND APPLICATIONS
Chairs: Christophe Tretz, Richard Brown

8:00am 5.1 Dynamic-Vt, Dual-Power-Supply SRAM Cell using D2G-SOI for Low-Power SoC Application
M. Yamaoka, K. Osada, K. Itoh, R. Tsuchiya, T. Kawahara; Central Research Laboratory, Hitachi, Ltd.

8:20am 5.2 Temperature Compensated Reference Circuits for SOI
S.C. Terry[1], S. Chen[1], B.J. Blalock[1], J.R. Jackson[1], B.M. Dufrene[1,2], M.M. Mojarradi[3], S.K. Islam[1], M.N. Ericson[4]; [1]University of Tennessee, [2]IBM Burlington, [3]Jet Propulsion Laboratory, [4]Oak Ridge National Laboratory

8:40am 5.3 Integrated Dynamic Body Contact for H-gate PD-SOI MOSFETs for High Performance/Low Power
J. Damiano, P.D. Franzon; North Carolina State University

9:00am 5.4 Accurate Current Mirroring in the Presence of Gate Leakage Current
F. H. Gebara[1], S. M. Martin[1], K. Nowka[2], R. B. Brown[1]; [1]University of Michigan, [2]Austin Research Labs, IBM

9:20am 5.5 Low Voltage and Performance Tunable CMOS Circuit Design Using Independently Driven Double Gate MOSFETs
A. Kumar, B. A. Minch, S. Tiwari; Cornell University

9:40am 5.6 Novel High-Density Low-Power High-Performance Double-Gate Logic Techniques
M.H. Chiang[1], K. Kim[2], C. Tretz[3], C.T. Chuang[2]; [1]National Ilan University, [2]IBM T.J. Watson Research Center, [3]IBM Engineering & Technology Services

Please also see Session 5 posters P5.1, P5.2

SESSION 6 NOVEL MATERIALS, PROCESSES, AND DEVICES
Chairs: Atsushi Ogura, Thierry Poiroux

10:20am 6.1 Fabrication and Characteristics of Novel Load PMOS SSTFT (Stacked Single-crystal Thin Film Transistor) for 3-Dimensional SRAM Memory Cell
Y.H. Kang, S.M. Jung, J.H. Jang, J.H. Moon, W.S. Cho, C.D. Yeo, K.H. Kwak, B.H. Choi, B.J. Hwang, W. R. Jung, S.J. Kim, J. H. Kim, J.H. Na, H. Lim, J.H. Jeong, K. Kim; Samsung Electronics Co., Ltd.

10:40am 6.2 Demonstration of Charge-Coupled Devices in Fully Depleted SOI
J.P Sage, V. Bolkhovsky, W.D. Oliver, D.D. Santiago, T.J. Weir; Lincoln Laboratory Massachusetts Institute of Technology

11:00am 6.3 Back-Floating Gate Non-Volatile Memory
U. Avci[1], A. Kumar[2], S. Tiwari[2]; [1]Applied and Engineering Physics, [2]Cornell University

11:20am 6.4 Low Temperature Silicon Circuit Layering For 3-Dimensional Integration
S. K. Kim, L. Xue, S. Tiwari; Cornell University

11:40am 6.5 Mobility Enhancement of SSOI Devices Fabricated with Sacrificial Thin Relaxed SiGe
J.J. Lee, J.S. Maa, D. J. Tweet, S.T. Hsu; Sharp Labs of America

12:00pm 6.6 Strained-Si/SiGe-on-Insulator Wafers Fabricated by Ge-Condensation Process
N. Hirashita[1], T. Numata[1], T. Tezuka[1], N. Sugiyama[1], K. Usuda[1], T. Irisawa[1], A. Tanabe[1], Y. Moriyama[1], S. Nakaharai[1], S. Takagi[2], E. Toyoda[3], Y. Miyamura[4]; [1]MIRAI-ASET, [2]MIRAI-AIST, [3]Toshiba Ceramics, [4]KEM

Please also see Session 6 posters P6.1

Thursday, October 7th

SESSION 7 DEVICE CHARACTERICATION, MODELING AND SIMULATION
Chairs: Dimitris Ioannou, Mike Liu

8:00am 7.1 Bulk Inversion in FinFETs and the Implied Insignificance of the Effective Gate Width
S.H. Kim, J.G. Fossum, V.P. Trivedi; University of Florida

8:20am 7.2 Technique for Rapid, In-Line Characterization of Switching History in Partially Depleted SOI Technologies
D. J. Pearson[1], M.B. Ketchen[1], M. Bhushan[2]; [1]IBM Thomas J. Watson Research Center, [2]IBM Server Group

8:40am 7.3 Unusual Floating Body Effect in Fully Depleted MOSFETs
M. Bawedin[1,2], S. Cristoloveanu[1], D. Flandre[2]; [1]IMEP, ENSERG, [2]Microelectronics Lab. (DICE), UCL

9:00am 7.4 New Magnetoresistance Method for Mobility Extraction in Scaled Fully-Depleted SOI Devices
C. Gallon[1], C. Fenouillet-Beranger[2], Y.M. Meziani[3], J.P. Cesso[3], J. Lusakowski[3], F. Teppe[3], N. Dyakonova[3], A. Vandooren[4], W. Knap[3], G. Ghibaudo[5], D. Delille[1], S. Cristoloveanu[5], T. Skotnicki[1]; [1]STMicroelectronics, [2]CEA LETI, [3]GES, Université Montpellier II, [4]Freescale Semiconductor, [5]IMEP

9:20am 7.5 History-Effect-Conscious SPICE Model Extraction for PD-SOI Technology
J.S. Goo, J.X. An, C. Thuruthiyil, T. Ly, Q. Chen, M. Radwin, Z.Y. Wu, M.S.L. Lee, L. Zamudio, J. Yonemurea, F. Assad, M.M. Pelella, A.B. Icel; Advanced Micro Devices.

9:40am 7.6 Compact Modeling of the Self Heating Effect in 120nm Multifinger Body-tacted SOI MOSFET for RF circuits
M. Reyboz, R. Daviot, O. Rozeau, P. Martin, M. Paccaud; LETI/CEA

Please also see Session 7 posters P7.1, P7.2 P7.3, P7.4, P7.5

SESSION 8 ANALOG, MIXED MODE, AND RF
Chairs: Ted Houston, Hector Sanchez

10:20am 8.1 A Low-Voltage Swing Latch for Reduced Power Dissipation in High-Frequency Microprocessors
P.F. Lu, L. Sigal, N. Cao, P. Woltgens, R. Robertazzi, D. Heidel; IBM T.J. Watson Research Center

10:40am 8.2 Small-and Large-Signal RF Characterization of Fully-Depleted Accumulation-mode Varactors for Low-Voltage LC-VCO SOI Design
B. Parvais[1], P. Delatte[2], H. Matsuhashi[3], F. Ichikawa[3], P. Simon[1], D. Schreurs[4], D. Flandre[1], J.P. Raskin[1]; [1]Université catholique de Louvain, [2]CISSOID, [3]Silicon Solutions Company, OKI Electric Co., Ltd. [4]Katolieke Universiteit Leuven

11:00am 8.3 A Very Low On-resistance SOI BiCDMOS LSI for Automotive Actuator Control
M. Hattori[1], F. Itoh[1], M. Kako[2]; [1]Toyota Motor Corp., [2]Aisan Industry Co., Ltd

11:20am 8.4 10GHz Low Phase Noise Fully Integrated VCOs in 130nm High Resistivity CMOS/SOI for 40Gbits/s Datacom
D. Axelrad[1], E. de Foucauld[1], P. Vincent[1], M. Belleville[1], F. Gaffiot [2]; [1]CEA-LETI, CEA Grenoble, [2]LEOM-UMR

11:40am 8.5 Analysis and Design of Digital CMOS Circuits in Hybrid SOI-Epitaxial Technology with Different Crystal Orientations
K. K. Das[1], S.H. Lo[1], C.T. Chuang[1], K. Bernstein[1], R. Williams[2]; [1]IBM T.J. Watson Research Center, [2]IBM Microelectronics Division

12:00pm 8.6 High-Temperature, Low-Power 8-Meg Ω by 1.2 MegHz SOI-CMOS Transimpedance Amplifier for MEMS-Based Wireless Sensors
L. Toygur, X. Yu, S. Garverick; Case Western Reserve University

Please also see Session 8 posters P8.1, P8.2

SESSION 9 **DEVICES - DOUBLE GATE**
Chairs: J.P. Colinge, Shigeru Kawanaka

1:20pm 9.1 Experimental Gate Misalignment Analysis on Double Gate SOI MOSFETs
J. Widiez[1,2], F. Daugé [3], M. Vinet[1], T. Poiroux[1], B. Previtali[1], M. Mouis[3], S. Deleonibus[1]; [1]CEA/DRT-LETI, [2]ST Microelectronics, [3]IMEP-ENSERG

1:40pm 9.2 CMOS Vertical Multiple Independent Gate Field Effect Transistor - MIGFET
L. Matthew, Y. Du, A.V.Y. Thean, M. Sadd, A. Vandooren, C. Parker, T. Stephens, R. Mora, R. Rai, M. Zavala, D. Sing, S. Kalpat, J. Hughes, R. Shimer, S. Jallepalli, G. Workman, B.E. White, B.Y. Nguyen, J. Mogab; APRDL, Motorola Inc.

2:00pm 9.3 Novel Process for Fully Self-Aligned Planar Ultrathin Body Double-Gate FET
R.S. Shenoy, K.C. Saraswat; Stanford University

2:20pm 9.4 Source/Drain-Doping Engineering for Optimal Nanoscale FinFET Design
V.P. Trivedi, J.G. Fossum; University of Florida

2:40pm 9.5 Full/Partial Depletion Effects in FinFETs
W. Xiong[1], C. R. Cleavelin[1], R. Wise[1], S. Yu[1], M. Pas[1], R.J. Zaman[2], M. Gostkowski[2], K. Matthews[2], C. Maleville[3], P. Patruno[3], T.J. King[4], J.P. Colinge ; [1]SiTD, Texas Instruments Incorporated [2]International Sematech, [3]SOITEC S.A., [4]University of California, Berkeley [5]University of California, Davis

3:00pm 9.6 DGSOI devices operated as velocity modulation transistors
F. Gamiz[1], C. Sampedro[1], A. Godoy[1], M. Prunnila[2], J. Ahopelto[2]; [1]Universidad de Granada, [2]VTT Information Technology

Please also see Session 9 posters P9.1, P9.2 P9.3

SESSION 10 **LATE NEWS**
3:40pm *Chair: Michael Mendicino*

ADDITIONAL AGENDA & SOCIAL FUNCTIONS

❖ **LATE NEWS - Thursday, 3:40pm**
Submission for the Late News Session will be accepted until August 13, 2004. Presentation of selected late papers will be on Thursday afternoon. Late News papers are not eligible for the Best Paper Award.

❖ **POSTER SESSION - Tuesday, 3:30 - 5:30pm**
Authors will be available for questions. Posters will be on display from Tuesday, 5:30pm until Thursday, 12:00pm

❖ **RUMP SESSION - Wednesday, 8pm**
As the technology for double- or multi-gate transistor structures mature and conventional partially-depleted (PD)/SOI (and bulk-Si) is aggressively scaled, the window to insert an advanced fully-depleted (FD)/SOI transistor architecture into a high-performance transistor roadmap is squeezed. A panel of distinguished experts will be assembled to discuss the technology, material, scalability, and performance issues of our industry's future transistor roadmap with a focus on the following theme: **Readiness of Double-Gate Transistors: Is there a window for UT/FD SOI?**

❖ **WELCOME RECEPTION - Monday, 6:00pm**
Please join us for the kick-off event of the conference. We have planned an evening of good snacks, good drinks, and good company–all we need is you to make it complete!

❖ **CONFERENCE BANQUET - Tuesday, 7:00pm**
Our banquet speaker this year is Dr. Fred Bernache of Freescale Semiconductor, Transportation and Standard Products Group. Dr. Bernache's topic will be the substantial technology infusion in automotive electronics and what it means to the consumer in the coming years.

❖ **COOKOUT - Wednesday, 6:30pm**
Combine great food and great networking with the great outdoors, and you have the conference "cookout"– a casual dinner under beautiful South Carolina skys. A great way to prepare for the Rump Session to follow!

EXPLORING CHARLESTON

Charleston, South Carolina
Where History Meets the Sea

Charleston! What grand images come to mind. The colonial Charles Towne as a wealthy growing city, Charleston during the rise and fall of Southern aristocracy before the American Civil War and the trauma and upheaval after the war ended. Out of the need for survival came the preservation of all that remained after natural and man-made destruction hit the city time and time again. Like no other city, Charleston has been described as a "living museum."

Parts of the city appear frozen in time; block after block of old downtown structures have been preserved and restored for residential and commercial use, and some brick and cobblestone streets remain. Despite the emphasis on preservation Charleston is culturally vibrant. The city nurtures theater, dance, music, and visual arts. There is fishing, golf and tennis, beautiful beaches, and island getaways. A gracious 300-year-old port city which is a living historical site that pays homage to its past, celebrates its present and moves gracefully into the future.

For more information on Charleston and what it has to offer, visit the Convention and Visitor's Bureau online at www.charlestoncvb.com. If you have specific needs, you can also reach the Charleston CVB via their toll free phone number (800) 868-8118. If you would like to write to them, their address is: Charleston Area CVB, P.O. Box 975, Charleston, SC 29402.

❖ **WEDNESDAY AFTERNOON TOURS**
Magnolia Plantation and Gardens Tour Package

There are many ways to experience the 300 years of history surrounding Charleston. For a taste of the "old South," we have arranged for transportation, entry into the Magnolia Plantation & Gardens park, a boxed lunch, and a choice of one of the two most popular tours in the park.

Overlooking the Ashley River, the Magnolia Plantation house is the 3rd version of the original plantation home and was built in 1865 after the 2nd version was burnt to the ground by General Sherman during the American Civil

War. The splendid English style gardens surrounding the house and extending into the 50 acres of the park are a result of 300 years of devotion by the Drayton family and their commitment to leaving more beauty in the world than when they first found it.

A choice of one of the following tours is included in our package:

1) HOUSE TOUR (approx. 1/2 hour) - The house is furnished in museum quality antiques and is considered the largest and finest collection of Early American furniture in the US.

2) NATURE TRAIN (approx. 45 minutes) **–** A narrated tram tour of the wildlife areas rice fields, & lakes with local wildlife.

You must indicate which tour you prefer when purchasing your tickets.

The bus will leave the hotel at 12:45pm (1245) and bring you into the Magnolia Plantation park where a box lunch will be provided. Both the House Tour & the Nature Train will begin at 2:00pm (1400).

After the 2:00pm tour (included with the price of your ticket), you are on your own to explore the park, relax, or take an additional tour (cost is extra). There are boat tours of the swamps and brochures available for those who wish to walk through the gardens on their own. The bus will return to the hotel at 4:30pm (1630) in plenty of time to enjoy the evening cookout.

If you decide to take a second tour (price not included with your conference tour package), it is highly recommended that you purchase your ticket before you attend the first tour to ensure you have a space on the second tour.

Space is limited for the Magnolia Plantation & Gardens tour package and it is recommended that your purchase your tour package tickets well in advance of the conference.

❖ **WEATHER:** Expect cool to warm days between 55 - 75 degrees with cool nights. October makes for changeable weather, so be prepared with warm weather clothing as well as a good jacket or coat. Dressing in layers is a good way to always be prepared for any temperature, even cool hotel rooms.

HOTEL SERVICES AND POLICIES

The conference hotel is the Francis Marion Hotel, 387 King Street, Charleston, South Carolina 29403. To make a reservation, please call (843)722-0600 or (877)756-2121 before 5:00pm EST September 3, 2004. Be sure to say you are with the IEEE International SOI Conference to get our group rate. You can also access the hotel's website at www.francismarionhotel.com

Opened in 1924, The Francis Marion Hotel was the largest and grandest in the Carolinas, and recently restored is once again Charleston's Grand Hotel. Rising 12 stories above the historic district, many of the Hotel's guestrooms offer spectacular views of Charleston's church steeples, antebellum mansions and famous harbor. Located downtown on historic Marion Square, the magnificent gardens, house museums, antique shops, local boutiques, restaurants and nightlife that make Charleston unique, are all an easy walk from the Hotel.

❖ **HOTEL POLICIES & RESERVATIONS**

The hotel has discounted room rates for conference attendees of $125 single or double occupancy. Rooms should be reserved as soon as possible to ensure availability at the discounted rate. This special rate is available until Friday, September 3, 2004 at 5:00pm. Please identify yourself as an IEEE International SOI Conference attendee when making your reservation. A limited number of rooms are available at the prevailing Government rate to qualified attendees.

Reservations can be made by calling either (843)722-0600 or (877)756-2121. You may also fax the hotel reservation form to (843)723-4633 Attn: Reservations. Check in time is 4:00pm and checkout time is 12:00pm.

A deposit must accompany all reservations in order to confirm the reservation. The deposit may be made by check, money order, or credit card. The deposit will be applied to the first night of your stay.

Hotel parking is available at the prevailing rate of $14 plus tax for valet service where fees can be charged to your room and $10 for self-parking, which must be paid directly to the parking garage in cash.

AREA AIRPORTS, CARRIERS, & RAILWAYS

❖ **NEAREST AIRPORT:**

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5500 International Blvd., #101
Charleston, SC 29413-6911
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Served By:

Continental Airlines • www.continental.com
Reservations: (800)525-0280

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Reservations: (800)221-1212

Northwest Airlines • www.nwa.com
Reservations: (800)225-2525

U.S. Airways
www.usairways.com
Reservations: (800)428-4322

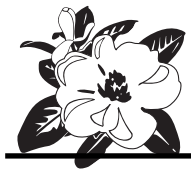
United Express • www.ual.com
Reservations: (800)241-6522

❖ **AIRPORT SHUTTLES:**

All shuttle rates from the airport is $10.00 per person. Taxi rate for one or two passengers to the Francis Marion Hotel is $20.00.

❖ **RAIL SERVICE:**

If you would like to take the scenic route without having to drive, call Amtrak for information and reservations at (800) 872-7245 Amtrak's web site is www.amtrak.com. Click on "reservations" to purchase tickets in advance. If you check out the "Rail Sale" selection, you will find the latest special rates.



RENTAL CARS DRIVING DIRECTIONS

❖ **CAR RENTAL:**

Alamo Rent A Car .....(800) 327-9633
Avis Car Rentals .....(800) 331-703
Budget Car Rental .....(800) 527-0700
Hertz Car Rental .....(800) 654-3131
National Car Rental....(800) 227-7368

❖ **DRIVING DIRECTIONS:**

Please be aware that the hotel has parking across the street at the prevailing rate of $14.00 plus tax for valet service where fees can be charged to your room and $10 for self-parking, which must be paid directly to the parking garage in cash.

From Interstate 26-West
(Charleston International Airport):

Follow I-26 heading east taking the Meeting Street Exit (please make sure not to take the North Meeting Street Exit). Proceed on Meeting Street, heading toward downtown. Turn right onto John Street. Proceed up John Street to King Street. Turn left onto King Street. The Francis Marion Hotel will be on the right, just passed St. Matthew's Lutheran Church.

From Hwy. 17 South-Kiawah/Seabrook/Savannah:

Follow Hwy. 17 heading north crossing the Ashley River Bridge (the "round" Holiday Inn will be on the left). Staying in the left lane and crossing over the overpass, proceed and bear right onto Cannon Street, which ends at King Street. Turn right onto King Street. Follow King Street to just past the Lutheran Church. The Westin Francis Marion will be on the right.

From Hwy. 17 North - Mt. Pleasant/Wild Dunes:

Follow Hwy. 17 heading south crossing the Cooper River Bridge. Before the first stoplight, bear left and take the King Street Exit. At the Stop sign, turn right onto King Street Follow King Street just passed the Lutheran Church. The Westin Francis Marion will be on the right.

CONFERENCE REGISTRATION

❖ **ON-SITE CONFERENCE REGISTRATION SCHEDULE**

Sunday, October 3	6:00pm - 8:00pm
Monday, October 4	7:00am - 5:00pm
Tuesday, October 5	7:00am - 5:00pm
Wednesday, October 6	7:00am - Noon
Thursday, October 7	7:00am - Noon

❖ **TO REGISTER:**

- Use the enclosed registration form or download a PDF form from our web site.
- Complete the registration form. Please fill-in all information completely.
- Mail or fax your registration form and payment no later than September 20, 2004:

IEEE International SOI Conference
520 Washington Blvd., #350
Marina del Rey, CA 90292 USA
310/305-1038

- Telephone registration is not available.
- Do not send your hotel reservation form with the conference registration form; send the hotel reservation form to the hotel.
- Please remember to include payment with your mailed or faxed form as only forms accompanied by payment will be accepted. There are no exceptions. You may pay for your registration with either check or credit card.
- While payment may be made via bank transfer, it is discouraged and there is an additional $25 fee per transfer.
- If you cannot mail or fax your form and your payment by September 20, 2004 you must register on-site at the conference (see On-site Registration Schedule).

❖ **TO PAY BY CREDIT CARD:**

Complete the registration form including the Credit Card Information section and either fax it to 310/305-1038 or mail it to 2004 IEEE International Conference, c/o BACM, 520 Washington Blvd., #350, Marina del Rey, CA 90292. Please be sure that the credit card information is complete, legible, and includes your signature.

❖ **TO PAY BY CHECK**:

Complete the registration form and mail it with your check to 2004 International SOI Conference c/o BACM, 520 Washington Blvd., #350, Marina del Rey, CA 90292. Please check payable to 2004 IEEE SOI Conference. All checks must be drawn on a US bank and in US funds only.

❖ **CANCELLATIONS:**

Cancellation requests must be made in writing to the conference manager. Refund requests received by September 20, 2004 will receive a refund of registration fees paid less a $25 processing fee. Requests received after September 20, 2004 will be considered by the committee. All refunds will be processed after the conference.

❖ **INCLUDED MEALS**

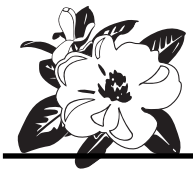
- **Short Course/Tutorial attendees:**
  Continental breakfast & lunch on Monday
- **Conference attendees:**
  Monday - Welcome Reception

  Tuesday - Continental breakfast & dinner with reception

  Wednesday - Continental breakfast & "Cook-Out" dinner

  Thursday - Continental breakfast

Please note: You are on your own for lunch Tuesday, Wednesday, and Thursday, as well as for dinner on Monday.



ADDITIONAL INFORMATION

For additional conference and registration information please contact:

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Marina del Rey, CA 90292
Tel.: 310.305.7885 Fax: 310.305.1038
e-mail: bobbi@bacminc.com

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www.francismarionhotel.com

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2004 IEEE SOI CONFERENCE REGISTRATION FORM

NAME TO APPEAR ON BADGE

*LAST NAME, FIRST NAME, MIDDLE INITIAL

*COMPANY OR AGENCY

*PREFERRED MAILING ADDRESS *MAIL STOP

*CITY/STATE/ZIP/COUNTRY

* TELEPHONE NUMBER *FAX NUMBER

*E-MAIL ADDRESS IEEE MEMBER NUMBER

REGISTRATION FEES

Advance Registration Fees apply to completed forms and payment received by September 20, 2004

Conference

	IEEE Member	Non IEEE Member	
Advance	$375	$450	
Regular	$420	$500	

Short Course Tutorial

	IEEE Member	Non IEEE Member	
Advance	$320	$400	
Regular	$350	$425	

Conference (Student):**

	IEEE Member	Non IEEE Member	
Advance	$210	$275	
Regular	$240	$305	

Short Course Tutorial (Student):**

	IEEE Member	Non IEEE Member	
Advance	$100	$155	
Regular	$130	$185	

$ _____

Registration Total

* As you want it to appear on the Conference List of Attendees

** For student registration, please complete:

School Attending: _____

Graduation Year: _____

ACTIVITIES

NOT INCLUDED IN CONFERENCE FEE

Magnolia Plantation Tour - Choose One

❑ with House Tour (Includes Lunch) . . . _____ @ $35 ea. = $_____

❑ with Boat Tour (Includes Lunch). . . . . _____ @ $35 ea. = $_____

ADDITIONAL PURCHASES

EXTRA SOCIAL FUNCTION TICKETS

(1 ticket to each event already included in Registration Fee)

Extra Banquet. . . . . _____ @ $45 ea. = $_____

Extra Cookout . . . . . _____ @ $45 ea. = $_____

ADDITIONAL CONFERENCE DIGESTS

(1 Digest already included in Conference Fee)

IEEE Member . . . . . _____ @ $40 ea. = $_____

Non-Member . . . . . _____ @ $50 ea. = $_____

Total Activities/Additional Fees

$ _____

Total Registration Fees $ _____

TOTAL ENCLOSED $ _____

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Mail check and completed form to:
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Please complete the following for credit card payment only:
Charge registration fees to my:

❑ American Express ❑ MasterCard ❑ VISA Card

CARD NUMBER

NAME AS IT APPEARS ON CREDIT CARD (PLEASE PRINT)

CARDHOLDER'S SIGNATURE EXP. DATE

Payment **must** accompany registration. Registrations without payment will not be accepted. Wire transfers must be approved in advance and are subject to a $25 fee. No telephone registrations available.

Do you have any special needs?

YES: _____

For additional information, please contact Conference Manager:
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(310) 305-7885 • Fax (310) 305-1038 • sandy@bacminc.com

HOTEL ACCOMMODATIONS FORM
2004 IEEE SOI INTERNATIONAL CONFERENCE
October 4 ~ 7, 2004

Cut off Registration Form and send this completed Hotel Accommodations form to:

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If calling, make sure to let the hotel know you are with the IEEE SOI Conference to get our group rate.
Hotel web site: www.francismarioncharleston.com

Rates for Single or Double Occupancy: $125

RESERVE EARLY: Reservations received after September 3, 2004 will be on a space and rate available basis only.
A major credit card is required to secure your room reservation.

NAME (PLEASE PRINT)

COMPANY

ADDRESS

CITY/STATE/ZIP/COUNTRY

TELEPHONE/FAX NUMBER

Arrival Date: _____ Departure Date: _____

Number of Persons: _____ Roommate Arrival Date: _____

Preferences: ❑ Smoking ❑ Non-smoking
❑ 1 King Size Bed ❑ 2 Double Beds

❑ American Express ❑ MasterCard ❑ VISA Card

CARD NUMBER EXP. DATE

NAME AS IT APPEARS ON CARD (PLEASE PRINT)

CARDHOLDER'S SIGNATURE

To receive your confirmation number by e-mail, please fill in your e-mail address: _____

Cancellation Policy:
To receive a refund on room reservations, cancellations must be received 3 days prior to scheduled arrival by close of business, 5pm EDT.